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Revision History

Document No.	Version.	Description	Date
305264	002	Added Intel® 915GME and 910GMLE chipsets.	April 2007
305264	001	Initial Release	January 2005

Mobile Intel 915PM Express Chipset Product Features

- The Intel® Pentium® M Processor with 2-MB L2 Cache processor support
 - 533-MHz processor system bus support
- Intel® Pentium® M Processor Low Voltage support
- Intel® Pentium® M Processor Ultra Low Voltage support
 - 400-MHz processor system bus support
 - Source Synchronous Double-pumped (2×) Address
 - Source Synchronous Quad-pumped (4×) Data
 - Supports front side bus (FSB) interrupt delivery
 - Host bus dynamic bus inversion HDVIN (DBI) support
 - 32-bit host bus addressing support
 - 12-deep in-order queue support
 - AGTL+ bus driver technology with integrated termination resistors supported
 - DPWR# signal to processor for FSB power management
 - BSEL pins for BCLK frequency select
 - Enhanced Intel SpeedStep® technology
- Intel® Celeron® M 90 nm processor support
- Intel® Celeron® M 90 nm processor ULV support
 - 400-MHz processor system bus support
 - Source Synchronous Double-pumped (2×) Address
 - Source Synchronous Quad-pumped (4×) Data
 - Supports front side bus (FSB) interrupt delivery
 - Host bus dynamic bus inversion HDVIN (DBI) support
 - 32-bit host bus addressing support
 - 12-deep in-order queue support
 - AGTL+ bus driver technology with integrated termination resistors supported
 - DPWR# signal to processor for FSB power management
 - BSEL pins for BCLK frequency select
- System Memory Support
 - DDR or DDR2 SDRAM channels (64-bits wide) are supported.
 - Supports SO-DIMM's of the same type (i.e. all DDR or all DDR2), not mixed.
 - 256-Mb, 512-Mb and 1-Gb technology supported using x8 or x16 devices.
 - Supports High Density memory Package for DDR or DDR2 type devices
 - Minimum memory supported is 128 MB
 - Maximum memory supported is 2 GB.
 - Supports configurations defined in the JEDEC* DDR / DDR2 SO-DIMM specification only
 - DDR feature support:
 - DDR – 333 MHz memory device
 - DDR2 feature support:
 - DDR2 - 400 MHz memory devices
 - DDR2 - 533 MHz memory devices
 - Supports On Die Termination (ODT) for DDR2



- — One memory channel organizations is supported for DDR
 - — Single Channel Mode
- — Two memory channel organizations are supported for DDR2:
 - — Dual Channel Symmetric Mode
 - — Dual Channel Asymmetric Mode
- — Single channel configuration supports: One, two, three or four ranks supported
- — Dual channel configuration: One or two ranks supported on each channel
- — Supports a max of two, double-sided unbuffered SO-DIMM's (4 rows populated)
- — Burst length of 4 or 8 (configured by BIOS at boot time)
- — Supports opportunistic refresh scheme
- — Supports "Fast Chip Select" mode
- — Supports Partial Writes to memory using Data Mask signals (DM)
- — Two memory throttling schemes supported to selectively throttle reads and/or writes per rank.
 - — Throttling can be triggered by on-die thermal sensor
 - — Throttling can be triggered by preset read/write bandwidth limits

- PCI Express* Based Graphics Interface
 - — PCI Express Architecture support for external graphics devices
 - — PCI Express Based Graphics interface only supported at core voltage at 1.05V
 - — One 16-lane PCI Express port (x16 PCI Express port) intended for Graphics Attach
 - — Fully compliant to the PCI Express Base Specification revision 1.0a
 - — Base PCI Express frequency support of 2.5 GB/s only
 - — Raw bit-rate on the data pins of 2.5 Gb/s, resulting in a raw bandwidth per pair of 250 MB/s given the 8b/10b encoding used to transmit data across this interface
 - — Automatic discovery, negotiation, and training of link out of reset
 - — Supports traditional PCI style traffic (asynchronous snooped, PCI ordering)
 - — Supports traditional AGP style traffic (asynchronous non-snooped, PCI-X Relaxed ordering)
 - — Hierarchical PCI-compliant configuration mechanism for downstream devices (i.e., normal PCI 2.3 Configuration space as a PCI-to-PCI bridge
 - — PCI Express Graphics Extended Configuration Space.
 - — The first 256 bytes of configuration space alias directly to the PCI Compatibility configuration space.
 - — The remaining portion of the fixed 4 kB block of memory-mapped space above that (starting at 100h) is known as extended configuration space.
 - — PCI Express Enhanced Addressing Mechanism.
 - — Accessing the device configuration space in a flat memory mapped fashion.
 - — Uses a 100Mhz differential reference clock
 - — PCI Express power management support
 - — Supports both Native and Legacy Hot Plug and PME functions.
- PCI Express x1 Port Support
 - — One general PCI Express x1 port supported
 - — PCI Express Based Graphics interface and SDVO are not functional in this mode

* Other names and brands may be claimed as the property of others

- Direct Media Interface (DMI)
 - Chip-to-chip interface between GMCH and ICH6-M
 - Configurable as x2 or x4 DMI lanes.
 - 2 GB/s point-to-point DMI to ICH6 (1 GB/s each direction)
 - 100 MHz reference clock (shared with PCI Express Graphics Attach).
 - 32-bit downstream addressing
 - APIC and MSI interrupt messaging support.
 - Message Signaled Interrupt (MSI) messages
 - SMI, SCI and SERR error indication
- System Interrupts
 - Supports both 8259 and Pentium M processor FSB interrupt delivery mechanisms.
- Power Management
 - SMRAM space remapping to A0000h (128 kB)
 - Supports extended SMRAM space above 256 MB, additional 1 MB TSEG from top of memory, cacheable (cache ability controlled by CPU)
 - Supports Suspend to System Memory (S3-Hot and S3-Cold supported), Suspend to Disk (S4) and Soft Off (S5)
 - ACPI 1.0b, 2.0 support
- Package
 - Micro – FCBGA
 - Package size: 37.5mm x 40mm
 - Die size: 395 x 395 mils
 - Ball pitch: 42 mil
 - Ball count: 1257

Mobile Intel 915GM Express Chipset Features

Note: All features for the Mobile Intel 915PM Express Chipset are supported on the Mobile Intel 915GM. Only additional integrated graphics features will be shown here.

- Integrated Display Interface support
 - Analog CRT DAC interface support
 - Supports max DAC frequency up to 400 MHz
 - 24-bit RAMDAC support
 - DDC2B compliant
 - Up to 2048 x 1536 mode support
 - Digital LVDS interface support
 - Compliant with ANSI/TIA/EIA -644-2001 spec
 - Integrated dual channel LVDS interface supported on Display Pipe B only
 - Supports 25 to 112 MHz single/dual channel LVDS interface:
 - Single channel LVDS interface support: 1 x 18 bpp
 - Dual channels LVDS interface support: 2 x 18 bpp
 - TFT panel type supported
 - Maximum Panel size supported up to UXGA
 - Maximum Wide panel size supported up to WUXGA
 - Ambient Light Sense support for automatic backlight brightness adjustments
 - Intel Display Power Savings Technology 2.0 support
 - Supports Single pipe simultaneous display with the CRT DAC and the LVDS ports under the following conditions:
 - Timings must match for both display
 - Panel Fitting. Panning, and Center mode supported
 - Spatial Dithering support to emulate up to 16 million colors for 18bpp TFT panels.
 - Spread spectrum clocking (SSC) supported
 - Supports down and center SSC via an SSC clock from an external SSC clock chip.
 - Supports down spread of – 2.5% or center spread of ± -1.25% in reference 30-50 kHz modulation rate
 - SSC must be disabled for LVDS port and CRT DAC single pipe simultaneous display mode.
 - Panel Power Sequencing support
 - Power down state can be either zero volt or high impedance
 - Integrated PWM interface for LCD Backlight Inverter Control
 - Analog TV-Out Interface support

- Integrated TV-out device supported on Display pipe A and pipe B.
- Three Integrated 10 bit DAC
- NTSC/PAL encoder standard formats supported
- Up to 1024x768 resolution supported for NTSC/PAL
- HDTV graphics resolutions support
- 480p/720p/1080i/1080p modes supported
- Multiplexed Output interface:
 - Composite Video
 - S-Video
 - Component Video (YprPb)
 - Combination: (Composite & S-Video)
- Macrovision support
- Overscan Scaling Support

- Serial Digital Video Output (SDVO) support
 - Two SDVO ports are supported
 - Supports a variety display devices such as DVI, TV Out, LVDS, etc.
 - Compliant with DVO specification 1.0 when combined with a DVI compliant external device and connector.
 - Data sourced from either display Pipe A or Pipe B
 - Supports single pipe simultaneous display with the DAC or LVDS ports
 - Timings must match for both display
 - Single pipe not supported with SSC on LVDS port
 - Each SDVO Port support display pixel rates up to 200 MP/s (600MB/s)
 - Fast point-to-point GMBUS is provided for SDVO device control
 - Supports Hot Plug and Display
 - Support for HDCP SDVO devices

- Internal Graphics Features
 - DVMT 3.0 support
 Max memory allocation support based on total system memory
 1-MB or 8 MB of pre-allocated memory supported
 - Intel® Dual-Frequency Graphics Technology
 - Intel® Smart 2D Display Technology
 - Asynchronous Display core and Render core clocks supported
 - 2D Display core frequency required to be equal or greater than 3D Render Core Frequency.
 - 2D Display core frequency at 133 or 190/200 MHz @ Vcc=1.05 V depending on the host/memory configurations
 - 3D Render core frequency at 133, 160/166 or 190/200 MHz @ Vcc=1.05 V depending on the host/memory configurations
 - 2D Display core frequency at 133, 200 or 333MHz @ Vcc=1.5 V depending on the host/memory configurations
 - 3D Render core frequency at 133, 160/166, 200 or 333 MHz @ Vcc=1.5 V depending on the host/memory configurations
 - Dual Independent display pipes.
 - 32 bit Hardware cursor supported

- 2D graphics engine
 - Optimized 256-bit BLT engine
 - Alpha Stretch Blitter
 - Anti-aliased Lines
 - 32-bit Alpha Blended Cursor
 - Color Space Conversion
 - Programmable 3-Color Transparent Cursor
 - 8-, 16- and 32-bit per pixel color
 - 8 ROP support
- High Quality 3D Setup and Render Engine
 - Setup matching processor geometry delivery rates
 - Triangle lists, strips and fans
 - Indexed vertex and flexible vertex formats
 - Vertex cache
 - Pixel accurate fast scissoring and clipping operation
 - Backface culling
 - Supports D3D and OGL pixelization rules
 - Sprite points
 - Shadow maps
 - Double-sided stencil
 - Zone Rendering 2.0 support
- High Quality Texture Engine
 - 533 MegaTexel/Sec Performance – 266 Mpixel/Sec fill rate up to 2 bilinear textures
 - Hardware Pixel Shader 2.0
 - Per-pixel perspective corrected texture mapping
 - 2/10/10/10 texture format
 - Bi-cubic filtering
 - Single-pass quad texture compositing
 - Enhanced texture blending functions
 - 12 levels of detail mip map sizes from 1x1 to 2Kx2K
 - All texture formats including 32-bit RGBA and 8-bit palettes
 - Alpha and luminance maps
 - Texture color-keying/chromakeying
 - Bilinear, trilinear and anisotropic mip-mapped filtering
 - Cubic environment reflection mapping
 - Embossed and DOT3 bump-mapping
 - DXTn and FXT1 texture decompression
 - Non-power of 2 texture
 - Render to texture

- 3D Graphics Rendering Enchantments
 - 1.3 Dual Texture GigaPixel/Sec Fill Rate
 - Flat and Gouraud Shading
 - Color Alpha Blending for Transparency
 - Vertex and Programmable Pixel Fog and Atmospheric Effects
 - Color Specular Lighting
 - Z Bias Support
 - Dithering
 - Anti-Aliased Lines
 - 16- and 24-bit Z Buffering
 - 8-bit Stencil Buffering
 - Double and Triple Render Buffer Support
 - 16- and 32-bit Color
 - Destination Alpha
 - Maximum 3D Resolution Supported: 1600x1200x32
 - Fast Clear Support
- Video DVD / PC-VCR support
 - HW Motion Compensation for MPEG2
 - Dynamic Bob and Weave Support for Video Streams
 - Resolution up to 1920x1080 with 2 vertical taps
 - Source Software DVD At 30 fps, Full Screen
 - Supports 720x480 DVD Quality Encoding at low CPU Utilization for PC-VCR or home movie recording and editing
- Video Overlay
 - Process Amplifier Color Control
 - Single High Quality Scalable Overlay
 - Multiple Overlay Functionality provided via Stretch Blitter (PIP, Video Conferencing, etc.)
 - 5-tap Horizontal, 2-tap Vertical Filtered Scaling
 - Independent Gamma Correction
 - Independent Brightness/Contrast/Saturation
 - Independent Tint/Hue Support
 - Destination Color-keying
 - Source Chroma-keying
 - Maximum Source Resolution: 720x480x32
 - Video Mixer Render (VMR)

Mobile Intel 915GMS Express Chipset Features

Note: All features for Mobile Intel 915GM Express Chipset is supported on Mobile Intel 915GMS. The differences are noted in this section.

- Intel® Pentium® M Processor Low Voltage support
- Intel® Pentium® M Processor Ultra Low Voltage support
- Intel® Celeron® M 90 nm processor ULV support
 - 400 MHz processor system bus support only
- System Memory Support
 - DDR2 memory channels (64-bits wide) are supported.
 - No DDR support
 - DDR2 feature support:
 - DDR2 – 400 memory devices
 - One memory channel organizations is supported:
 - Single Channel mode
- PCI Express* Based Graphics Interface not supported
- Integrated Display Interface support
 - Digital LVDS interface support
 - Integrated single channel LVDS interface supported on Display Pipe B only
 - Supports 25 to 112 MHz single channel LVDS interface:
 - Single channel LVDS interface support: 1 x 18 bpp
 - Maximum Panel size supported up to SXGA+ (single channel only)
 - Wide panel size supported up to WXGA (single channel only)
 - Serial Digital Video Output (SDVO) support
 - One SDVO port is supported
 - SDVO B
- Internal Graphics Features
 - Graphics core voltage support's 1.05 V only
 - 2D Display core frequency at 133 or 200 MHz @ Vcc = 1.05 V
 - 3D Render core frequency at 133 or 160 MHz @ Vcc = 1.05 V
- Package
 - Micro – FCBGA
 - Package size: 27 x 27 mm
 - Die size: 395 x 395 mils
 - Ball pitch: See the mechanical drawing
 - Ball count: 840

Mobile Intel 910GML Express Chipset Product Features

Note: All features for the Mobile Intel 915GM Chipset are supported on the Intel 910GML unless otherwise noted in this section.

- Intel® Celeron® M 90 nm processor support
- Intel® Celeron® M 90 nm processor ULV support
 - 400 MHz processor system bus support only
- System Memory Support
 - DDR or DDR2 SDRAM channels (64-bits wide) are supported.
 - DDR - 333 MHz memory device
 - Single Channel Memory support for DDR 333
 - DDR2 - 400 MHz memory devices
 - Dual Channel Memory configuration support for DDR2 400
- PCI Express* Based Graphics Interface not supported
- Integrated Display Interface support
 - Digital LVDS interface support
 - Max Panel size supported is SXGA+
 - Analog TV-Out Interface support
 - HDTV graphics mode is not supported.
- Internal Graphics Features
 - 2D Display core frequency support from 133 MHz & 190/200 MHz @ Vcc = 1.05 / 1.5 V depending on Host/Memory configuration
 - 3D Render core frequency support from 133 MHz & 160/166 MHz @ Vcc = 1.05 / 1.5 V depending on Host/Memory configuration



Mobile Intel 915GME Express Chipset Features

Note: All features for the Mobile Intel 915GM Express Chipset are supported on the Intel 915GME unless otherwise noted in this section.

- Macrovision copy protection technology has been disabled on the Intel 915GME.
- The TV-out port has been disabled on the Intel 915GME. Please ensure platform design guide recommendations for TV-out disabling have been followed.

Mobile Intel 910GMLE Express Chipset Features

Note: All features for the Mobile Intel 910GML Express Chipset are supported on the Intel 910GMLE unless otherwise noted in this section.

- Macrovision copy protection technology has been disabled on the Intel 910GMLE.
- The TV-out port has been disabled on the Intel 910GMLE. Please ensure platform design guide recommendations for TV-out disabling have been followed.

§

1 Introduction

This document is the datasheet for the Mobile Intel® 915GM/PM/GMS/GME and 910GML/GMLE Express chipset families.

1.1 Overview

The Mobile Intel 915GM/PM/GMS/GME & 910GML/GMLE Express chipset family is a graphics memory controller hub (GMCH) designed for use with the Intel Pentium M Processor with 2 MB L2 Cache and Intel® Celeron® M processor 90 nm. The family includes the following chipsets:

- Mobile Intel 915GM Express chipset supports Intel Graphics Media Accelerator 900 and PCI Express* based Graphics
- Mobile Intel 915PM Express chipset supports PCI Express based Graphics only
- Mobile Intel 915GMS Express chipset supports Intel Graphics Media Accelerator 900 in small form factor package
- Mobile Intel 910GML Express chipset supports Intel Graphics Media Accelerator 900
- Mobile Intel 915GME Express chipset supports Intel Graphics Media Accelerator 900 and PCIExpress* based graphics with TV-out and Macrovision copy protection technology disabled.
- Mobile Intel 910GMLE Express chipset supports Intel Graphics Media Accelerator 900 with TV-out and Macrovision copy protection technology disabled.

Note: Intel 915GMS may have notes in GRAY-20% shade throughout this document. This is to point out differences which may be specific only for this chipset.

The GMCH provides high-performance, integrated graphics and manages the flow of information. The Intel 915GM chipset adds enhancements for the following areas:

- System Memory (DDR / DDR2)
- PCI Express Based Graphics (discrete graphics devices)
- Intel Graphics enhancements:
 - DVMT 3.0 support
 - Zone Rendering 2.0 support
 - Quad pixel pipe rendering engine
 - Pixel Shader 2.0 support
 - 4x Faster Setup Engine
- Serial Digital Video Output (SDVO)
- TV Out Support
 - HDTV resolution support
- LVDS support
 - Wide panel support
 - Ambient Light Sense support for automatic backlight brightness adjustments
 - Intel Display Power Savings Technology 2.0 support
 - Integrated PWM interface for LCD Backlight Inverter Control
- Direct Media Interface (DMI)

1.1.1 System Memory Interface

The GMCH integrates a system memory DDR/DDR2 controller with two, 64-bit wide interfaces. Only Double Data Rate (DDR / DDR2) memory is supported; consequently, the buffers support DDR SSTL_2 and DDR2 SSTL_18 signaling interfaces. The memory controller interface is fully configurable through a set of control registers.

Three system memory modes of operation supported are:

- Single Channel mode
- Dual Channel Asymmetric mode
- Dual Channel Symmetric mode

1.1.2 PCI Express* Based Graphics and Intel SDVO Interface

The GMCH multiplexes a PCI Express Graphics interface with two Intel SDVO ports. The SDVO ports can each support a single-channel SDVO device. If both ports are active in single-channel mode, they can have different display timing and data. Alternatively the SDVO ports can combine to support dual channel devices, supporting higher resolutions and refresh rates.

PCI Express Based Graphics Interface

The GMCH contains one 16-lane (x16) PCI Express port intended for an external PCI Express Based graphics card. The PCI Express port is fully compliant to the PCI Express Base Specification revision 1.0a. The x16 port operates at a data rate of 2.5 GB/s while employing 8b/10b encoding. This allows a maximum theoretical bandwidth of 40 GB/s each direction. Intel 915GM/ PM may also be configured as PCI Express x1 port.

1.1.3 Display Interface

Note: Analog TV interface not supported on the Intel 915GME and Intel 910GMLE chipsets.

The GMCH is capable of driving a CRT, LCD panel, Analog TV and/or two SDVO devices (SDVO ports are muxed with PCI Express).

The display is the defining portion of a graphics controller. The display converts a set of source images or surfaces, combines them and sends them out at the proper timing to an output interface connected to a display device. Along the way, the data can be converted from one format to another, stretched or shrunk, and color corrected or gamma converted.

1.1.4 SDVO Interface

The GMCH supports two SDVO ports multiplexed with PCI Express Graphics interface. The SDVO ports are capable of driving a variety of external TV-Out, TMDS, and LVDS transmitter devices. SDVO devices are capable of driving a standard progressive scan analog monitor with resolutions up to 2048x1536 at 75 Hz. This interface may be configured for as PCI Express x1 port also.

1.1.5 DMI

DMI is a point -to- point connection from the GMCH to the ICH6-M.

1.2 Terminology

Term	Description
AGTL+	Advanced Gunning Transceiver Logic + (AGTL+) bus
AGP	Accelerated Graphics Port refers to the AGP/PCI interface in previous generation chipset. It have been replaced by PCI Express * based graphics interface
ALS	Ambient Light Sensor
GMCH	Refers to the Graphics Memory Controller Hub chipset component for Intel 910GML and Intel 915GM Chipset.
MCH	Refers to the Memory Controller Hub chipset component for Intel 915PM MCH Chipset. Any references to GMCH will also apply to MCH unless otherwise noted.
bpp	Bit per pixel
Beacon	30 kHz–500 MHz signal used by PCI Express to exit the L2 power state.
Bit Clock	The nominal data rate that information is passed on an Interface. Note that in the PCI Express interface this clock is embedded within the data and is not a separate signal.
BLI	Backlight Inverter
Bridge	A Device which virtually or actually connects a PCI/PCI Express segment or PCI Express Port with an internal Component interconnect or another PCI/PCI-X segment or PCI Express Port. A Bridge must include a software configuration interface as described in this document.
Core	The internal base logic in the Mobile Intel® 915 Express Chipset Family
CPU	Central Processing Unit
CRT	Cathode Ray Tube
DBL	Display Brightness Link
DDC	Display Data Channel (VESA standard)
DDR	Double Data Rate SDRAM memory technology
DDR2	Second generation Double Data Rate SDRAM memory technology
DINV (DBI)	Dynamic Bus inversion
DMI	Direct Media Interface. The chip-to-chip inter-connect between the Mobile Intel 915 Express Chipset Family GMCH and the ICH6-M, is an Intel Proprietary interface.
DPMS	Display Power Management Signaling (standard created by VESA)
DPST	Intel® Display Power Savings Technology
DVI*	Digital Visual Interface is the interface specified by the DDWG (Digital Display Working Group) DVI Spec. Rev. 1.0
DVMT	Dynamic Video Memory Technology
EDID	Extended Display Identification Data
EIST	Enhanced Intel SpeedStep technology
FSB	Front Side Bus, synonymous with Host or CPU bus.
Full Reset	A Full GMCH Reset is defined in this document when RSTIN# is asserted.
GTL+	Gunning Transceiver Logic + (GTL+) bus
Host	This term is used synonymously with processor
HDTV	High Definition Television
I2C	Inter-IC (a two wire serial bus created by Philips)
Intel ICH6-M	The Intel® I/O Controller Hub component that contains the primary PCI interface, LPC interface, USB2, ATA-100, and other I/O functions. It communicates with the GMCH over a proprietary interconnect called DMI.
IGD	Integrated Graphics Device

Term	Description
INTx	An interrupt request signal where X stands for interrupts A,B,C and D
IPI	Inter Processor Interrupt
LCD	Liquid Crystal Display.
LFP	Local Flat Panel
LVDS	Low Voltage Differential Signaling: - A high speed, low power data transmission standard used for display connections to LCD panels.
MSI	Message Signaled Interrupt. MSI allow a device to request interrupt service via a standard memory write transaction instead of through a hardware signal. A transaction initiated outside the host, conveying interrupt information to the receiving agent through the same path that normally carries read and write commands.
NCTF	Non-Critical to Function: As a function of Intel's continuous improvement goals, we have identified package level modifications that add to the overall solder joint strength and reliability of our component. Through our research and development, we have concluded that adding non-critical to function (NCTF) solder balls to our packages can improve the overall package-to-board solder joint strength and reliability. Ball locations/signal ID's followed with the suffix of “NCTF” have been designed into the package footprint to enhance the package to board solder joint strength/reliability of this product by absorbing some of the stress introduced by the Characteristic Thermal Expansion (CTE) mismatch of the Die to package interface. It is expected that in some cases, where board stresses are excessive, these balls may crack partially or completely, however, cracks in the NCTF balls will have no impact to our product performance or reliability. Intel has added these balls primarily to serve as stress absorbers.
NTSC	National Television Standards Committee
PAL	Phase Alternate Line
SDTV	Standard Definition Television
PCI Express*	PCI Express* Interface is based on the *PCI Express Specification 1.0a*
PCI Express Based Graphics	PCI Express Based Graphics. External Graphics using PCI Express* Architecture. A high-speed serial interface whose configuration is software compatible with the existing PCI specifications. The specific PCI Express implementation intended for connecting the GMCH to an external graphics controller is an x16 link and replaces AGP.
Primary PCI	The physical PCI bus that is driven directly by the ICH component. Communication between Primary PCI and the GMCH occurs over DMI. Note that the Primary PCI bus is **not** PCI Bus 0 from a configuration standpoint.
FSB	Processor System Bus. Connection between Mobile Intel® 915 Express Chipset Family GMCH and the CPU. Also known as the Host interface
PWM	Pulse Width Modulation
Rank	A unit of DRAM corresponding 4 to 8 devices in parallel, ignoring ECC. These devices are usually, but not always, mounted on a single side of a SO-DIMM.
SCI	System Control Interrupt. Used in ACPI protocol.
SDVO	Serial Digital Video Out (SDVO). Digital display channel that serially transmits digital display data to an external SDVO device. The SDVO device accepts this serialized format and then translates the data into the appropriate display format (i.e., TMDS, LVDS, TV-Out). This interface is not electrically compatible with the previous digital display channel - DVO. For Mobile Intel® 915 Express Chipset Family, it will be multiplexed on a portion of the x16 graphics PCI Express interface.

Term	Description
SDVO Device	Third party codec that utilizes SDVO as an input. May have a variety of output formats, including DVI, LVDS, HDMI, TV-out, etc.
SERR	An indication that an unrecoverable system error has occurred on an I/O bus.
SMI	System Management Interrupt. Used to indicate any of several system conditions such as thermal sensor events, throttling activated, access to System Management RAM, chassis open, or other system state related activity.
SSC	Spread Spectrum Clocking
TMDS	Transition Minimized Differential Signaling. Signaling interface from Silicon Image that is used in DVI and HDMI.
TOLM	Top Of Low Memory. The highest address below 4GB for which a CPU initiated memory read or write transaction will create a corresponding cycle to DRAM on the memory interface.
UMA	Unified Memory Architecture. Describes Mobile Intel® 915 Express Chipset Family GMCH using system memory for its graphics frame buffers.
VCO	Voltage Controlled Oscillator
VDL	Video Data Link
×1	Refers to a Link or Port with one Physical Lane.
x8	Refers to a Link or Port with eight Physical Lanes.
xN	Refers to a Link with “N” Physical Lanes.
VRM	Video Render Mixer
VTT	Processor Side Bus power supply (VCCP)

1.3 Reference Documents

Document	Location
Intel® Pentium® M Processor with 2 MB L2 Cache and 533 MHz Front Side Bus Datasheet	http://developer.intel.com
Intel® Pentium® M Processor on 90 nm Process with 2 MB L2 Cache Datasheet	http://developer.intel.com
Intel® Celeron® M Processor on 90 nm Process Datasheet	http://developer.intel.com
PCI Express Base Specification 1.0a	http://www.pcisig.org/
VESA Specifications	http://www.vesa.org
PCI Local Bus Specification 2.3	http://www.pcisig.com
Advanced Configuration and Power Management(ACPI) Specification 1.0b & 2.0	http://www.teleport.com/~acpi/
JEDEC Double Data Rate (DDR) SDRAM Specification *JEDEC Double Data Rate 2 (DDR2) SDRAM Specification*	http://www.jedec.com
Intel Developer website link for DDR validation information	http://developer.intel.com/technology/memory/
Intel Developer website link for PCI Express Architecture*	http://www.intel.com/technology/pciexpress/devnet/mobile.htm

2 Signal Description

This section describes the GMCH signals. These signals are arranged in functional groups according to their associated interface. The following notations are used to describe the signal type:

I Input pin

O Output pin

I/O Bi-directional Input/Output pin

The signal description also includes the type of buffer used for the particular signal:

AGTL+ Open Drain AGTL+ interface signal. Refer to the AGTL+ I/O Specification for complete details. (VCCP)

PCIE PCI Express interface signals. These signals are compatible with PCI Express Base Specification 1.0a Electrical Signal Specifications. The buffers are not 3.3-V tolerant. Differential voltage spec = (|D+ - D-|) * 2 = 1.2 V max. Single-ended maximum = 1.5 V. Single-ended minimum = 0 V. Please refer to the PCIE specification.

CMOS CMOS buffers. 1.5 V tolerant

HVCMOS CMOS buffers. 2.5 V tolerant

COD CMOS Open Drain buffers. 2.5 V tolerant

DDR DDR system memory (2.5 V CMOS buffers)

DDR2 DDR2 system memory (1.8 V CMOS buffers)

SSTL-2 2.5 V Stub Series Termination Logic

SSTL-1.8 1.8 V Stub Series Termination Logic

A Analog reference or output. May be used as a threshold voltage or for buffer compensation

LVDS Low Voltage Differential Signal interface

Ref Voltage reference signal

Note: System Address and Data Bus signals are logically inverted signals. The actual values are inverted of what appears on the system bus. This must be considered and the addresses and data bus signals must be inverted inside the GMCH. All processor control signals follow normal convention: A 0 indicates an active level (low voltage), and a 1 indicates an active level (high voltage).

2.1 Host Interface

Unless otherwise noted, the voltage level for all signals in this interface is tied to the termination voltage of the host bus (VCCP).

Note: Host interfaces signal group is supported on the Intel 915GM, Intel 915PM, Intel 915GMS, Intel 915GME, Intel 910GML and Intel 910GMLE chipsets.

2.1.1 Host Interface Signals

Signal Name	Type	Description
HADS#	I/O AGTL+	**Host Address Strobe:** The system bus owner asserts HADS# to indicate the first of two cycles of a request phase. The GMCH can also assert this signal for snoop cycles and interrupt messages.
HBNR#	I/O AGTL+	**Host Block Next Request:** Used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the CPU bus pipeline depth.
HBPRI#	O AGTL+	**Host Bus Priority Request:** The GMCH is the only Priority Agent on the system bus. It asserts this signal to obtain the ownership of the address bus. This signal has priority over symmetric bus requests and will cause the current symmetric owner to stop issuing new transactions unless the HLOCK# signal was asserted.
HBREQ0#	I/O AGTL+	**Host Bus Request 0#:** The GMCH pulls the processor bus HBREQ0# signal low during HCPURST#. The signal is sampled by the processor on the active-to-inactive transition of HCPURST#. HBREQ0# should be tri-stated after the hold time requirement has been satisfied.
HCPURST#	O AGTL+	**Host CPU Reset:** The CPURST# pin is an output from the GMCH. The GMCH asserts HCPURST# while RSTIN# is asserted and for approximately 1 ms after RSTIN# is deasserted. HCPURST# allows the processor to begin execution in a known state.
HDBSY#	I/O AGTL+	**Host Data Bus Busy:** Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
HDEFER#	O AGTL+	**Host Defer:** Signals that the GMCH will terminate the transaction currently being snooped with either a deferred response or with a retry response.
HDINV[3:0]#	I/O AGTL+	**Host Dynamic Bus Inversion:** Driven along with the HFD[63:0]# signals. Indicates if the associated signals are inverted or not. HDINVF[3:0]# are asserted such that the number of data bits driven electrically low (low voltage) within the corresponding 16-bit group never exceeds 8. **HDINV# — Data Bits** HDINV[3]# — HD[63:48]# HDINV[2]# — HD[47:32]# HDINV[1]# — HD[31:16]# HDINV[0]# — HD[15:0]#
HDRDY#	I/O AGTL+	**Host Data Ready:** Asserted for each cycle that data is transferred.

Signal Name	Type	Description
HA[31:3]#	I/O AGTL+ 2X	**Host Address Bus:** HA[31:3]# connects to the CPU address bus. During processor cycles the HA[31:3]# are inputs. The GMCH drives HA[31:3]# during snoop cycles on behalf of DMI. HA[31:3]# are transferred at 2x rate. Note that the address is inverted on the CPU bus.
HADSTB[1:0]#	I/O AGTL+ 2X	**Host Address Strobe:** HA[31:3]# connects to the CPU address bus. During CPU cycles, the source synchronous strobes are used to transfer HA[31:3]# and HREQ[4:0]# at the 2x transfer rate. **Strobe** — **Address Bits** HADSTB[0]# — HA[16:3]#, HREQ[4:0]# HADSTB[1]# — HA[31:17]#
HD[63:0]#	I/O AGTL+ 4X	**Host Data:** These signals are connected to the CPU data bus. HD[63:0]# are transferred at 4x rate. Note that the data signals are inverted on the CPU bus depending on the HDINV[3:0]# signals.
HDSTBP[3:0]# HDSTBN[3:0]#	I/O AGTL+ 4X	**Host Differential Host Data Strobes:** The differential source synchronous strobes are used to transfer HD[63:0]# and HDINV[3:0]# at the 4x transfer rate. **Strobe** — **Data Bits** HDSTBP[3]#, HDSTBN[3]# — HD[63:48]#, HDINV[3]# HDSTBP[2]#, HDSTBN[2]# — HD[47:32]#, HDINV[2]# HDSTBP[1]#, HDSTBN[1]# — HD[31:16]#, HDINV[1]# HDSTBP[0]#, HDSTBN[0]# — HD[15:00]#, HDINV[0]#
HHIT#	I/O AGTL+	**Host Hit:** Indicates that a caching agent holds an unmodified version of the requested line. Also, driven in conjunction with HITM# by the target to extend the snoop window.
HHITM#	I/O AGTL+	**Host Hit Modified:** Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. Also, driven in conjunction with HIT# to extend the snoop window.
HLOCK#	I AGTL+	**Host Lock:** All CPU bus cycles sampled with the assertion of HLOCK# and HADS#, until the negation of HLOCK# must be atomic, i.e. *PCI Express graphics access* to System Memory is allowed when HLOCK# is asserted by the CPU.
HREQ[4:0]#	I/O AGTL+ 2X	**Host Request Command:** Defines the attributes of the request. HREQ[4:0]# are transferred at 2x rate. Asserted by the requesting agent during both halves of the Request Phase. In the first half the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second half the signals carry additional information to define the complete transaction type.
HTRDY#	O AGTL+	**Host Target Ready:** Indicates that the target of the processor transaction is able to enter the data transfer phase.

Signal Name	Type	Description
HRS[2:0]#	O AGTL+	**Host Response Status:** Indicates the type of response according to the following the table: **HRS[2:0]#** — **Response type** 000 — Idle state 001 — Retry response 010 — Deferred response 011 — Reserved (not driven by GMCH) 100 — Hard Failure (not driven by GMCH) 101 — No data response 110 — Implicit Write back 111 — Normal data response
HDPWR#	O AGTL+	**Host Data Power:** Used by GMCH to indicate that a data return cycle is pending within 2 HCLK cycles or more. CPU use's this signal during a read-cycle to activate the data input buffers in preparation for HDRDY# and the related data.
HCPUSLP#	O CMOS	**Host CPU Sleep:** When asserted in the Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts.

2.1.2 Host Interface Reference and Compensation

Signal Name	Type	Description
HVREF	I A	**Host Reference Voltage:** Reference voltage input for the Data, Address, and Common clock signals of the Host AGTL+ interface.
HXRCOMP	I/O A	**Host X RCOMP:** Used to calibrate the Host AGTL+ I/O buffers. This signal is powered by the Host Interface termination rail (VCCP).
HXSCOMP	I/O A	**Host X SCOMP**: Slew Rate Compensation for the Host Interface
HXSWING	I A	**Host X Voltage Swing:** These signals provide reference voltages used by the HXRCOMP circuits.
HYRCOMP	I/O A	**Host Y RCOMP**: Used to calibrate the Host AGTL+ I/O buffers.
HYSCOMP	I/O A	**Host Y SCOMP:** Slew Rate Compensation for the Host Interface
HYSWING	I A	**Host Y Voltage Swing:** These signals provide reference voltages used by the HYRCOMP circuitry.

2.2 DDR DRAM Interface

1. DDR DRAM interfaces signal group is supported the Intel 915PM, Intel 915GM, Intel 915GMS Intel 915GME, Intel 910GML and Intel 910GMLE chipsets, unless otherwise noted.
2. Intel 915GMS supports single channel only, therefore some signals may not be applicable.

2.2.1 DDR / DDR2 SDRAM Channel A Interface

Signal Name	Type	Description
SA_DQ[63:0]	I/O SSTL1.8 / 2 2x	**Data Bus:** DDR / DDR2 Channel A data signal interface to the SDRAM data bus. Single channel mode: Route to SO-DIMM 0 & SO-DIMM1 Dual channel mode: Route to SO-DIMM A
SA_DM[7:0]	O SSTL1.8 / 2 2X	**Data Mask:** These signals are used to mask individual bytes of data in the case of a partial write, and to interrupt burst writes. When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SA_DM[7:0] for every data byte lane. Single channel mode: Route to SO-DIMM 0 & SO-DIMM1 Dual channel mode: Route to SO-DIMM A
SA_DQS[7:0]	I/O SSTL1.8 2x	**Data Strobes:** DDR: The rising and falling edges of SA_DQS[7:0] are used for capturing data during read and write transactions. DDR2: SA_DQS[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SA_DQS[7:0] and its SA_DQS[7:0]# during read and write transactions. Single channel mode: Route to SO-DIMM 0 & SO-DIMM1 Dual channel mode: Route to SO-DIMM A
SA_DQS[7:0]#	I/O SSTL1.8 2x	**Data Strobe Complements** DDR1: No Connect. These signals are not used for DDR devices DDR2 : These are the complementary DDR2 strobe signals. Single channel mode: Route to SO-DIMM 0 & SO-DIMM1 Dual channel mode: Route to SO-DIMM A
SA_MA[13:0]	O SSTL1.8 / 2	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM. Single channel mode: Route to SO-DIMM 0 Dual channel mode: Route to SO-DIMM A Note: SA_MA13 is for support of 1 Gb devices.
SA_BS[2:0]	O SSTL1.8 / 2	**Bank Select**: These signals define which banks are selected within each SDRAM rank. Single channel mode: Route to SO-DIMM 0 Dual channel mode: Route to SO-DIMM A Note: SA_BS2 is for support for DDR2 only for 8 bank devices.

Signal Name	Type	Description
SA_RAS#	O SSTL1.8 / 2	**RAS Control signal**: Used with SA_CAS# and SA_WE# (along with SM_CS#) to define the SDRAM commands. Single channel mode: Route to SO-DIMM 0 Dual channel mode: Route to SO-DIMM A
SA_CAS#	O SSTL1.8 / 2	**CAS Control signal:** Used with SA_RAS# and SA_WE# (along with SM_CS#) to define the SDRAM commands. Single channel mode: Route to SO-DIMM 0 Dual channel mode: Route to SO-DIMM A
SA_WE#	O SSTL1.8 / 2	**Write Enable Control signal:** Used with SA_RAS# and SA_CAS# (along with SM_CS#) to define the SDRAM commands. Single channel mode: Route to SO-DIMM 0 Dual channel mode: Route to SO-DIMM A
SA_RCVENIN#	I SSTL1.8 / 2	**Clock Input:** Used to emulate source-synch clocking for reads. Connects internally to SA_RCVENOUT#. Leave as No Connect.
SA_RCVENOUT#	O SSTL1.8 / 2	**Clock Output:** Used to emulate source-synch clocking for reads. Connects internally to SA_RCVENIN#. Leave as No Connect.

2.2.2 DDR / DDR2 SDRAM Channel B Interface

Signal Name	Type	Description
SB_DQ[63:0]	I/O SSTL1.8 / 2 2x	**Data Lines**: DDR / DDR2 Channel B data signal interface to the SDRAM data bus. Single Channel mode: No connect. Dual channel mode: Route to SO-DIMM B **NOTE**: Signals do not exist in Intel 915GMS.
SB_DM[7:0]	O SSTL1.8 / 2 2X	**Data Mask:** When activated during writes, the corresponding data groups in the SDRAM are masked. There is one SB_DM[7:0] for every data byte lane. These signals are used to mask individual bytes of data in the case of a partial write, and to interrupt burst writes. Single Channel mode: No connect. Dual channel mode: Route to SO-DIMM B **NOTE**: Signals do not exist in Intel 915GMS.
SB_DQS[7:0]	I/O SSTL1.8 / 2 2x	**Data Strobes:** DDR: The rising and falling edges of SB_DQS[7:0] are used for capturing data during read and write transactions. DDR2: SB_DQS[7:0] and its complement signal group make up a differential strobe pair. The data is captured at the crossing point of SB_DQS[7:0] and its SB_DQS[7:0]# during read and write transactions. Single Channel mode: No connect. Dual channel mode: Route to SO-DIMM B **NOTE**: Signals do not exist in Intel 915GMS.
SB_DQS[7:0]#	I/O SSTL1.8 2x	**Data Strobe Complements** (DDR2 only): DDR1: No Connect. These signals are not used for DDR devices DDR2 : These are the complementary DDR2 strobe signals. Single Channel mode: No connect. Dual channel mode: Route to SO-DIMM B **NOTE**: Signals do not exist in Intel 915GMS.
SB_MA[13:0]	O SSTL1.8 / 2	**Memory Address:** These signals are used to provide the multiplexed row and column address to the SDRAM. Single channel mode: Route to SO-DIMM 1 Dual channel mode: Route to SO-DIMM B **NOTE**: SB_MA13 is for support of 1 Gb devices.
SB_BS[2:0]	O SSTL1.8 / 2	**Bank Select**: These signals define which banks are selected within each SDRAM rank. Single channel mode: Route to SO-DIMM 1 Dual channel mode: Route to SO-DIMM B **NOTE**: SB_BS2 is for DDR2 support only.
SB_RAS#	O SSTL1.8 / 2	**RAS Control signal**: Used with SB_CAS# and SB_WE# (along with SM_CS#) to define the SDRAM commands. Single channel mode: Route to SO-DIMM 1 Dual channel mode: Route to SO-DIMM B

Signal Name	Type	Description
SB_CAS#	O SSTL1.8 / 2	**CAS Control signal:** Used with SB_RAS# and SB_WE# (along with SM_CS#) to define the SDRAM commands. Single channel mode: Route to SO-DIMM 1 Dual channel mode: Route to SO-DIMM B
SB_WE#	O SSTL1.8 / 2	**Write Enable Control signal:** Used with SB_RAS# and SB_CAS# (along with SM_CS#) to define the SDRAM commands. Single channel mode: Route to SO-DIMM 1 Dual channel mode: Route to SO-DIMM B
SB_RCVENIN#	I SSTL1.8 / 2	**Clock Input:** Used to emulate source-synch clocking for reads. Leave as No Connect. **NOTE**: Signals do not exist in Intel 915GMS.
SB_RCVENOUT#	O SSTL1.8 / 2	**Clock Output:** Used to emulate source-synch clocking for reads. Leave as No Connect. **NOTE**: Signals do not exist in Intel 915GMS.

2.2.3 DDR / DDR2 Common Signals

Signal Name	Type	Description
SM_CK[1:0], SM_CK[4:3]	O SSTL1.8 / 2	**SDRAM Differential Clock:** The crossing of the positive edge of SM_CKx and the negative edge of its complement SM_CKx# are used to sample the command and control signals on the SDRAM. **SM_CK[0:1]** and its complement **SM_CK[1:0]#** signal make a differential clock pair output. Single channel mode: Route to SO-DIMM 0 Dual channel mode: Route to SO-DIMM A **SM_CK[4:3]** and its complement **SM_CK[4:3]#** signal make a differential clock pair output. Single channel mode: Route to SO-DIMM 1 Dual channel mode: Route to SO-DIMM B **NOTE**: **SM_CK2** and **SM_CK5** are reserved and not supported.
SM_CK[1:0]#, SM_CK[4:3]#	O SSTL1.8 / 2	**SDRAM Inverted Differential Clock:** These are the complementary Differential DDR2 Clock signals. **NOTE**: **SM_CK2#** and **SM_CK5#** are reserved and not supported.
SM_CS[3:0]#	O SSTL1.8 / 2	**Chip Select:** (1 per Rank): These signals select particular SDRAM components during the active state. There is one Chip Select for each SDRAM rank **SM_CS[1:0]#** : Single channel mode: Route to SO-DIMM 0 Dual channel mode: Route to SO-DIMM A **SM_CS[3:2]#** : Single channel mode: Route to SO-DIMM 1 Dual channel mode: Route to SO-DIMM B
SM_CKE[3:0]	O SSTL1.8 / 2	**Clock Enable:** (1 per Rank): SM_CKE[3:0] is used: —To initialize the SDRAMs during power-up —To power-down SDRAM ranks —To place all SDRAM ranks into and out of self-refresh during STR. SM_CKE[1:0]: Single channel mode: Route to SO-DIMM 0 Dual channel mode: Route to SO-DIMM A SM_CKE[3:2]: Single channel mode: Route to SO-DIMM 1 Dual channel mode: Route to SO-DIMM B
SM_ODT[3:0]	O SSTL1.8	**On Die Termination: Active Termination Control**. (DDR2 only) SM_ODT[1:0]: Single channel mode: Route to SO-DIMM 0 Dual channel mode: Route to SO-DIMM A SM_ODT[3:2]: Single channel mode: Route to SO-DIMM 1 Dual channel mode: Route to SO-DIMM B DDR: Leave as no connects. Not used for DDR devices. DDR2: On-die termination for DDR2 devices.

2.2.4 DDR SDRAM Reference and Compensation

Signal Name	Type	Description
SMRCOMPN	I/O A	**System Memory RCOMP N**: Buffer compensation This signal is powered by the System Memory rail (2.5 V for DDR, 1.8 V for DDR2).
SMRCOMPP	I/O A	**System Memory RCOMP P**: Buffer compensation This signal is powered by the System Memory rail
SMXSLEWIN	I A	**X Buffer Slew Rate Input control.**
SMXSLEWOUT	O A	**X Buffer Slew Rate Output control.**
SMYSLEWIN	I A	**Y Buffer Slew Rate Input control.**
SMYSLEWOUT	O A	**Y Buffer Slew Rate Output control.**
SMVREF[1:0]	I A	**SDRAM Reference Voltage:** Reference voltage inputs for each DQ, DQS, & RCVENIN#. Also used during ODT RCOMP.
SMOCDCOMP[1:0]	I A	**On-Die DRAM OCD driver compensation** OCD compensation

2.2.4.1 DDR / DDR2 Common Signal Mapping

Table 2-1. Single Channel Mode Signal Mapping for DDR/DDR2

Single Channel Signal Mapping	
SO-DIMM 0	**SO-DIMM 1**
SM_CK [1:0]	SM_CK [4:3]
SM_CK# [1:0]	SM_CK# [4:3]
SM_CS# [1:0]	SM_CS# [3:2]
SM_CKE [1:0]	SM_CKE [3:2]
SM_ODT[1:0] (DDR2 support only)	SM_ODT [3:2] (DDR2 support only)
SA_BS [2:0]	SB_BS[2:0]
SA_MA[13:0]	SB_MA [13:0]
SA_RAS#	SB_RAS#
SA_CAS#	SB_CAS#
SA_WE#	SB_WE#
SA_DQ [63:0]	
SA_DQS [7:0]	
SA_DQS#[7:0]	
SA_DM[7:0]	



Table 2-2. Dual Channel Mode Signal Mapping for DDR/DDR2

Dual Channel Mode	Channel A	Channel B
	SODIMM A	SODIMM B
SM_CK[1:0]	SM_CK[1:0]	NA
SM_CK[1:0]#	SM_CK[1:0]#	NA
SM_CK[4:3]	NA	SM_CK[4:3]
SM_CK[4:3]#	NA	SM_CK[4:3]#
SM_CS[1:0]#	SM_CS[1:0]#	NA
SM_CKE[1:0]	SM_CKE[1:0]	NA
SM_ODT[1:0] (DDR2 support)	SM_ODT[1:0] (DDR2 support)	NA
SM_CS[3:2]#	NA	SM_CS[3:2]#
SM_CKE[3:2]	NA	SM_CKE[3:2]
SM_ODT[3:2] (DDR2 support)	NA	SM_ODT[3:2] (DDR2 support)

2.3 PCI Express Based Graphics Interface Signals

Unless otherwise specified, these signals are AC coupled.

PCI Express Based Graphics is supported for Intel 915GM, Intel 915GME and Intel 915PM chipsets.

Signal Name	Type	Description
EXP_RXN[15:0] EXP_RXP[15:0]	I PCIE	PCI Express Receive Differential Pair
EXP_TXN[15:0] EXP_TXP[15:0]	O PCIE	PCI Express Transmit Differential Pair
EXP_ICOMPO	I A	PCI Express Output Current and Resistance Compensation
EXP_COMPI	I A	PCI Express Input Current Compensation

2.3.1 Serial DVO and PCI Express Based Graphics Signal Mapping

SDVO and PCI Express Interface for graphics architecture are muxed together. The following table shows the signal mapping.

SDVOB and SDVOC interfaces are supported for Intel 915GM, Intel 915GME, Intel 910GML and Intel 910GMLE chipsets.

SDVOB interface is supported for Intel 915GMS chipset as highlighted in GREY-20%.

Table 2-3. SDVO and PCI Express Based Graphics Port Signal Mapping

SDVO MODE	PCI Express MODE
SDVOB_RED#	EXP_TXN0
SDVOB_RED	EXP_TXP0
SDVOB_GREEN#	EXP_TXN1
SDVOB_GREEN	EXP_TXP1
SDVOB_BLUE#	EXP_TXN2
SDVOB_BLUE	EXP_TXP2
SDVOB_CLKN	EXP_TXN3
SDVOB_CLKP	EXP_TXP3
SDVOC_RED#	EXP_TXN4
SDVOC_RED	EXP_TXP4
SDVOC_GREEN#	EXP_TXN5
SDVOC_GREEN	EXP_TXP5
SDVOC_BLUE#	EXP_TXN6
SDVOC_BLUE	EXP_TXP6
SDVOC_CLKN	EXP_TXN7
SDVOC_CLKP	EXP_TXP7
SDVO_TVCLKIN#	EXP_RXN0
SDVO_TVCLKIN	EXP_RXP0
SDVOB_INT#	EXP_RXN1
SDVOB_INT	EXP_RXP1
SDVO_FLDSTALL#	EXP_RXN2
SDVO_FLDSTALL	EXP_RXP2
SDVOC_INT#	EXP_RXN5
SDVOC_INT	EXP_RXP5

2.4 DMI

DMI x2 or x4 is supported for Intel 915GM, Intel 915PM, Intel 915GME, Intel 910GML and Intel 910GMLE chipsets.

Signal Name	Type	Description
DMI_RXP[3:0] DMI_RXN[3:0]	I PCIE	**DMI input from ICH6-M:** Direct Media Interface receive differential pair
DMI_TXP[3:0] DMI_TXN[3:0]	O PCIE	**DMI output to ICH6-M:** Direct Media Interface transmit differential pair

DMI x2 is supported for Intel 915GMS chipset

Signal Name	Type	Description
DMI_RXP[1:0] DMI_RXN[1:0]	I PCIE	**DMI input from ICH6-M:** Direct Media Interface receive differential pair
DMI_TXP[1:0] DMI_TXN[1:0]	O PCIE	**DMI output to ICH6-M:** Direct Media Interface transmit differential pair

2.5 Integrated Graphics Interface Signals

The Integrated Graphics Interface signals in Section 2.5 are supported for the Intel 915GM, Intel 915GMS, Intel 915GME, Intel 910GML and the Intel 910GMLE chipsets. These signals are reserved for the Intel 915PM chipset.

Note: Please refer to the platform design guide for details for recommendation for these signal groups.

Note: Signals in section 2.5.2 are not supported on Intel 915GME and Intel 910GMLE chipsets.

2.5.1 CRT DAC Signals

Signal Name	Type	Description
RED	O A	**RED Analog Video Output**: This signal is a CRT Analog video output from the internal color palette DAC.
RED#	O A	**RED# Analog Output**: This signal is an analog video output from the internal color palette DAC. This signal is used to provide noise immunity.
GREEN	O A	**GREEN Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC.
GREEN#	O A	**GREEN# Analog Output**: This signal is an analog video output from the internal color palette DAC. This signal is used to provide noise immunity.
BLUE	O A	**BLUE Analog Video Output:** This signal is a CRT Analog video output from the internal color palette DAC.
BLUE#	O A	**BLUE# Analog Output:** This signal is an analog video output from the internal color palette DAC. This signal is used to provide noise immunity.
REFSET	O A	**Resistor Set**: Set point resistor for the internal color palette DAC. A 256-Ω ± 1% resistor is required between REFSET and motherboard ground.

Signal Name	Type	Description
HSYNC	O HVCMOS	**CRT Horizontal Synchronization:** This signal is used as the horizontal sync (polarity is programmable) or “sync interval”.
VSYNC	O HVCMOS	**CRT Vertical Synchronization**: This signal is used as the vertical sync (polarity is programmable).

2.5.2 Analog TV-out Signals

Note: Analog TV-out signals are not supported on the Intel 915GME and Intel 910GMLE chipsets. Please follow design guide recommendations to properly terminate these signals on the motherboard.

Signal Name	Type	Description
TVDAC_A	O A	**TVDAC Channel A Output:** TVDAC_A supports the following: **Composite**: CVBS signal **Component**: Chrominance (Pb) analog signal
TVDAC_B	O A	**TVDAC Channel B Output:** TVDAC_B supports the following: **S-Video**: Luminance analog signal **Component**: Luminance (Y) analog signal
TVDAC_C	O A	**TVDAC Channel C Output:** TVDAC_C supports the following: **S-Video**: Chrominance analog signal **Component**: Chrominance (Pr) analog signal
TV_IRTNA	O A	**Current Return for TVDAC Channel A:** Connect to ground on board
TV_IRTNB	O A	**Current Return for TVDAC Channel B:** Connect to ground on board
TV_IRTNC	O A	**Current Return for TVDAC Channel C:** Connect to ground on board
TV_REFSET	O A	**TV Resistor set:** TV Reference Current uses an external resistor to set internal reference voltage levels. A 5-kΩ ± 0.5% resistor is required between REFSET and motherboard ground.

2.5.3 LVDS Signals

Note: LVDS Channel B interface is not supported and do not exist for Intel 915GMS.

Signal Name	Type	Description
LDVS Channel A		
LADATAP[2:0]	I/O LVDS	Channel A differential data output - positive
LADATAN[2:0]	I/O LVDS	Channel A differential data output –negative
LACLKP	I/O LVDS	Channel A differential clock output – positive
LACLKN	I/O LVDS	Channel A differential clock output – negative
LDVS Channel B		
LBDATAP[2:0]	I/O LVDS	Channel B differential data output – positive **NOTE**: Signals do not exist in Intel 915GMS.
LBDATAN[2:0]	I/O LVDS	Channel B differential data output –negative **NOTE**: Signals do not exist in Intel 915GMS.
LBCLKP	I/O LVDS	Channel B differential clock output – positive **NOTE**: Signals do not exist in Intel 915GMS.
LBCLKN	I/O LVDS	Channel B differential clock output – negative **NOTE**: Signals do not exist in Intel 915GMS.
LFP Panel power and backlight control		
LVDD_EN	O HVCMOS	LVDS panel power enable: Panel power control enable control. This signal is also called VDD_DBL in the CPIS specification and is used to control the VDC source to the panel logic.
LBKLT_EN	O HVCMOS	LVDS backlight enable: Panel backlight enable control. This signal is also called ENA_BL in the CPIS specification and is used to gate power into the backlight circuitry.
LBKLT_CRTL	O HVCMOS	Panel backlight brightness control: Panel brightness control. This signal is also called VARY_BL in the CPIS specification and is used as the PWM Clock input signal.
LVDS Reference signals		
LIBG	I/O Ref	LVDS Reference Current. – 1.5 kΩ Pull down resistor needed
LVREFH	I Ref	Reserved. - No connect.
LVREFL	I Ref	Reserved. - No connect.
LVBG	O A	Reserve. - No connect

2.5.4 Serial DVO Interface

All of the pins in this section are multiplexed with the upper eight lanes of the PCI Express interface.

SDVOB and SDVOC interfaces are supported for Intel 915GM, Intel 915GME, Intel 910GML and Intel 910GMLE chipsets. SDVOB interface is supported for Intel 915GMS chipset as highlighted in GREY-20%.

Signal Name	Type	Description
SDVO B Interface		
SDVOB_CLKP	O PCIE	Serial Digital Video B Clock. Multiplexed with EXP_TXP_3.
SDVOB_CLKN	O PCIE	Serial Digital Video B Clock Complement. Multiplexed with EXP_TXN_3.
SDVOB_RED	O PCIE	Serial Digital Video B Red Data. Multiplexed with EXP_TXP_0.
SDVOB_RED#	O PCIE	Serial Digital Video B Red Data Complement. Multiplexed with EXP_TXN_0.
SDVOB_GREEN	O PCIE	Serial Digital Video B Green Data. Multiplexed with EXP_TXP_1.
SDVOB_GREEN#	O PCIE	Serial Digital Video B Green Data Complement. Multiplexed with EXP_TXN_1.
SDVOB_BLUE	O PCIE	Serial Digital Video B Blue Data. Multiplexed with EXP_TXP_2.
SDVOB_BLUE#	O PCIE	Serial Digital Video B Blue Data Complement. Multiplexed with EXP_TXN_2.
SDVO C Interface		
SDVOC_RED	O PCIE	Serial Digital Video C Red Data / SDVO B Alpha. Multiplexed with EXP_TXP_4. **NOTE**: Signals do not exist in Intel 915GMS.
SDVOC_RED#	O PCIE	Serial Digital Video C Red Complement / Alpha Complement. Multiplexed with EXP_TXN_4. **NOTE**: Signals do not exist in Intel 915GMS.
SDVOC_GREEN	O PCIE	Serial Digital Video C Green. Multiplexed with EXP_TXP_5. **NOTE**: Signals do not exist in Intel 915GMS.
SDVOC_GREEN#	O PCIE	Serial Digital Video C Green Complement. Multiplexed with EXP_TXN_5. **NOTE**: Signals do not exist in Intel 915GMS.
SDVOC_BLUE	O PCIE	Serial Digital Video Channel C Blue. Multiplexed with EXP_TXP_6. **NOTE**: Signals do not exist in Intel 915GMS.
SDVOC_BLUE#	O PCIE	Serial Digital Video C Blue Complement. Multiplexed with EXP_TXN_6. **NOTE**: Signals do not exist in Intel 915GMS.

Signal Name	Type	Description
SDVOC_CLKP	O PCIE	Serial Digital Video C Clock. Multiplexed with EXP_TXP_7. **NOTE**: Signals do not exist in Intel 915GMS.
SDVOC_CLKN	O PCIE	Serial Digital Video C Clock Complement. Multiplexed with EXP_TXN_7. **NOTE**: Signals do not exist in Intel 915GMS.
SDVO Common Signals		
SDVO_TVCLKIN	I PCIE	Serial Digital Video TVOUT Synchronization Clock. Multiplexed with EXP_RXP_0.
SDVO_TVCLKIN#	I PCIE	Serial Digital Video TV-out Synchronization Clock Complement. Multiplexed with EXP_RXN_0.
SDVO_FLDSTALL	I PCIE	Serial Digital Video Field Stall. Multiplexed with EXP_RXP_2.
SDVO_FLDSTALL#	I PCIE	Serial Digital Video Field Stall Complement. Multiplexed with EXP_RXN_2.
SDVOB_INT	I PCIE	Serial Digital Video Input Interrupt. Multiplexed with EXP_RXP_1.
SDVOB_INT#	I PCIE	Serial Digital Video Input Interrupt Complement. Multiplexed with EXP_RXN_1.
SDVOC_INT	I PCIE	Serial Digital Video Input Interrupt. Multiplexed with EXP_RXP_5.
SDVOC_INT#	I PCIE	Serial Digital Video Input Interrupt Complement. Multiplexed with EXP_RXN_5.

2.5.5 Display Data Channel (DDC) and GMBUS Support

Signal Name	Type	Description
LCTLA_CLK	I/O COD	I2C Based control signal (Clock) for External SSC clock chip control –
LCTLB_DATA	I/O COD	I2C Based control signal (Data) for External SSC clock chip control –
DDCCLK	I/O COD	CRT DDC clock monitor control support
DDCDATA	I/O COD	CRT DDC Data monitor control support
LDDC_CLK	I/O COD	EDID support for flat panel display
LDDC_DATA	I/O COD	EDID support for flat panel display
SDVOCTRL_CLK	I/O COD	I2C Based control signal (Clock) for SDVO device
SDVOCTRL_DATA	I/O COD	I2C Based control signal (Data) for SDVO device

2.6 PLL Signals

Note: PLL interfaces signal group are supported on the Mobile Intel 915GM/PM/GMS/GME and Intel 910GML/GMLE Express chipsets, unless otherwise noted.

Signal Name	Type	Description
HCLKP	I Diff Clk	**Differential Host Clock In**: Differential clock input for the Host PLL. Used for phase cancellation for FSB transactions. This clock is used by all of the GMCH logic that is in the Host clock domain. Also used to generate core and system memory internal clocks. This is a low voltage differential signal and runs at ¼ the FSB data rate.
HCLKN	I Diff Clk	**Differential Host Clock Input Complement:**
GCLKP	I Diff Clk	**Differential PCI Express based Graphics / DMI Clock In**: These pins receive a differential 100 MHz Serial Reference clock from the external clock synthesizer. This clock is used to generate the clocks necessary for the support of PCI Express.
GCLKN	I Diff Clk	**Differential PCI Express based Graphics / DMI Clock In complement**
DREF_CLKP	I Diff Clk	**Display PLLA Differential Clock In** – Display PLL Differential Clock In, no SSC support –
DREF_CLKN	I Diff Clk	**Display PLLA Differential Clock In Complement** – Display PLL Differential Clock In Complement - no SSC support
DREF_SSCLKP	I Diff Clk	**Display PLLB Differential Clock In** – Optional Display PLL Differential Clock In for SSC support – **NOTE**: Differential Clock input for optional SSC support for LVDS display.
DREF_SSCLKN	I Diff Clk	**Display PLLB Differential Clock In complement** – Optional Display PLL Differential Clock In Complement for SSC support **NOTE**: Differential Clock input for optional SSC support for LVDS display.

2.7 Reset and Miscellaneous Signals

Reset and Miscellaneous interfaces signal group is supported the Mobile Intel 915GM/PM/GMS/GME and Intel 910GML/GMLE Express chipsets, unless otherwise noted.

Signal Name	Type	Description
RSTIN#	I HVCMOS	**Reset In**: When asserted this signal will asynchronously reset the GMCH logic. This signal is connected to the PLT_RST# output of the ICH6-M. This input has a Schmitt trigger to avoid spurious resets. This input buffer is 3.3-V tolerant.
PWROK	I HVCMOS	**Power OK**: When asserted, PWROK is an indication to the GMCH that core power has been stable for at least 10 µs. This input buffer is 3.3-V tolerant.
H_BSEL [2:0] (CFG[2:0])	I HVCMOS	**Host Bus Speed Select:** At the deassertion of RSTIN#, the value sampled on these pins determines the expected frequency of the bus. External pull-ups are required.
CFG[17:3]	I AGTL+	**HW straps:** CFG [17:3] has internal pull up. **NOTE**: Not all CFG Balls are supported for Intel 915GMS.
CFG[20:18]	I HVCMOS	**HW straps:** CFG [20:18] has internal pull down **NOTE**: Not all CFG Balls are supported for Intel 915GMS.
BM_BUSY#	O HVCMOS	**GMCH Integrated Graphics Busy**: Indicates to the ICH that the integrated graphics engine within the MCH is busy and transitions to low power states should not be attempted until that is no longer the case.
THRMTRIP#	O COD	**GMCH Thermal Trip**: Assertion of THERMTRIP# (Thermal Trip) indicates the GMCH junction temperature has reached a level beyond which damage may occur. Upon assertion of THERMTRIP#, the GMCH will shut off its internal clocks (thus halting program execution) in an attempt to reduce the GMCH core junction temperature. To protect GMCH, its core voltage (Vcc) must be removed following the assertion of THERMTRIP#. Once activated, THERMTRIP# remains latched until RSTIN# is asserted. While the assertion of the RSTIN# signal will deassert THERMTRIP#, if the GMCH's junction temperature remains at or above the trip level, THERMTRIP# will again be asserted.
EXT_TS[1:0]#	I HVCMOS	**External Thermal Sensor Input**: If the system temperature reaches a dangerously high value then this signal can be used to trigger the start of system memory throttling. **NOTE**: EXT_TS1# functionality is not supported in 915GMS. A pull up is required on this pin

2.8 Power and Ground

Interface	Ball Name	Description
Host	VTT (VCCP)	FSB power supply (1.05 V) - (VCCP)
DRAM	VCCA_SM	VCCASM is the Analog power supply for SM data buffers used for DLL & other logic (1.5 V)
	VCCSM	System memory power supply (DDR=2.5 V; DDR2=1.8 V)
PCI Express Based Graphics / DMI	VCC3G	PCI Express / DMI Analog power supply (1.5 V)
	VCCA_3GBG	PCI Express / DMI band gap power supply (2.5 V)
	VSSA_3GBG	PCI Express / DMI band gap ground
PLL Analog	VCCA_HPLL	Power supply for the Host VCO in the host/mem/core PLL (1.5 V)
	VCCA_MPLL	Power supply for the mem VCO in the host/mem/core PLL (1.5 V)
	VCCD_HMPLL	Power Supply for the digital dividers in the HMPLL (1.5 V)
	VCCA_3GPLL	Power supply for the 3GIO PLL (1.5 V)
	VCCA_DPLLA	Display A PLL power supply (1.5 V)
	VCCA_DPLLB	Display B PLL power supply (1.5 V)
High Voltage Interfaces	VCCHV	Power supply for the HV buffers (2.5 V)
CRT DAC	VCCA_CRTDAC	Analog power supply for the DAC (2.5 V)
	VSSA_CRTDAC	Analog ground for the DAC
	VCC_SYNC	Power supply for HSYNC/ VSYNC (2.5 V)
LVDS	VCCD_LVDS	Digital power supply (1.5 V)
	VCCTX_LVDS	Data/Clk Tx power supply (2.5 V)
	VCCA_LVDS	LVDS analog power supply (2.5 V)
	VSSALVDS	LVDS analog VSS
TVDAC	VCCA_TVBG	TV DAC Band Gap Power (3.3 V)
	VSSA_TVBG	TV DAC Band Gap VSS
	VCCD_TVDAC	Dedicated Power Supply for TVDAC (1.5 V)
	VCCDQ_TVDAC	Power Supply for Digital Quiet TVDAC (1.5 V)
	VCCA_TVDACA	Power Supply for TV Out Channel A (3.3 V)
	VCCA_TVDACB	Power Supply for TV Out Channel B (3.3 V)
	VCCA_TVDACC	Power Supply for TV Out Channel C (3.3 V)
Core	VCC	Core VCC – (1.05 V or 1.5 V)
Ground	VSS	Ground
NCTF	**Non-Critical To Function power signals:** "NCTF" (Non-Critical To Function) have been designed into the package footprint to enhance the Solder Joint Reliability of our products by absorbing some of the stress introduced by the Characteristic Thermal Expansion (CTE) mismatch of the Die to package interface. It is expected that in some cases, these balls may crack partially or completely, however, this will have no impact to our product performance or reliability. Intel has added these balls primarily to serve as sacrificial stress absorbers. **NOTE**: Signals do not exist in Intel 915GMS.	
	VTT_NCTF	NCTF FSB power supply (1.05 V or 1.2 V)
	VCC_NCTF	NTCF Core VCC – (1.05 V or 1.5 V)
	VCCSM_NCTF	NTCF System memory power supply (DDR=2.5 V; DDR2=1.8 V)
	VSS_NCTF	NTCF Ground

2.9 Reset States and Pull-Up / Pull-Downs

This section describes the expected states of the GMCH I/O buffers during and immediately after the assertion of RSTIN#. This table only refers to the contributions on the interface from the GMCH and does not reflect any external influence (such as external pull-up/pull-down resistors or external drivers.

Legend:

DRIVE: Strong drive (to normal value supplied by the core logic if not otherwise stated)

TERM: Normal termination devices are turned on

LV: Low voltage

HV: High voltage

IN: Input buffer enabled

ISO: Isolate input buffer so that it doesn't oscillate if input left floating.

TRI: Tri-state

PU: Weak internal pull-up

PD: Weak internal pull-down

STRAP: Strap input sampled during assertion or on the deasserting edge of RSTIN#

2.9.1 Host Interface Signals

Unless otherwise noted, the voltage level for all signals in this interface is tied to the termination voltage of the host bus (VCCP).

Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3	PU/PD
HADS#	I/O AGTL+	TERM HV	TERM HV	TRI (No VTT)	
HBNR#	I/O AGTL+	TERM HV	TERM HV	TRI (No VTT)	
HBPRI#	O AGTL+	TERM HV	TERM HV	TRI (No VTT)	
HBREQ0#	I/O AGTL+	TERM HV	TERM HV	TRI (No VTT)	
HCPURST#	O CMOS	DRIVE LV	TERM HV after ~ 1ms	TRI (No VTT)	
HDBSY#	I/O AGTL+	TERM HV	TERM HV	TRI (No VTT)	
HDEFER#	O AGTL+	TERM HV	TERM HV	TRI (No VTT)	
HDINV[3:0]#	I/O AGTL+	TERM HV	TERM HV	TRI (No VTT)	
HDRDY#	I/O AGTL+	TERM HV	TERM HV	TRI (No VTT)	
HA[31:3]#	I/O AGTL+	TERM HV	TERM HV	TRI (No VTT)	
HADSTB[1:0]#	I/O AGTL+	TERM HV	TERM HV	TRI (No VTT)	
HD[63:0]#	I/O AGTL+	TERM HV	TERM HV	TRI (No VTT)	
HDSTBP[3:0]#	I/O AGTL+	TERM HV	TERM HV	TRI (No VTT)	
HDSTBN[3:0]#	I/O AGTL+	TERM HV	TERM HV	TRI (No VTT)	
HHIT#	I/O AGTL+	TERM HV	TERM HV	TRI (No VTT)	
HHITM#	I/O AGTL+	TERM HV	TERM HV	TRI (No VTT)	
HLOCK#	I/O AGTL+	TERM HV	TERM HV	TRI (No VTT)	
HREQ[4:0]#	I/O AGTL+	TERM HV	TERM HV	TRI (No VTT)	
HTRDY#	O AGTL+	TERM HV	TERM HV	TRI (No VTT)	
HRS[2:0]#	O AGTL+	TERM HV	TERM HV	TRI (No VTT)	
HDPWR#	O AGTL+	TERM HV	TERM HV	TRI (No VTT)	
HCPUSLP#	O CMOS	IN	IN		

2.9.2 Host Interface Reference and Compensation

Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3	PU/PD
HVREF	I A	IN	IN	TRI	
HXRCOMP	I/O A	TRI	TRI after RCOMP	TRI	
HXSCOMP	I/O A	TRI	TRI after RCOMP	TRI	
HXSWING	I A	IN	IN		
HYRCOMP	I/O A	TRI	TRI after RCOMP	TRI	
HYSCOMP	I/O A	TRI	TRI after RCOMP	TRI	
HYSWING	I A	IN	IN		

2.9.3 DDR / DDR2 SDRAM Channel A Interface

Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3	PU/PD
SA_DQ[63:0]	I/O SSTL1.8 / 2	TRI	TRI		
SA_DM[7:0]	O SSTL1.8 / 2	TRI	TRI		
SA_DQS[7:0]	I/O SSTL1.8	TRI	TRI		
SA_DQS[7:0]#	I/O SSTL1.8	TRI	TRI		
SA_MA[13:0]	O SSTL1.8 / 2	TRI	TRI		
SA_BS[2:0]	O SSTL1.8 / 2	TRI	TRI		
SA_RAS#	O SSTL1.8 / 2	TRI	TRI		
SA_CAS#	O SSTL1.8 / 2	TRI	TRI		
SA_WE#	O SSTL1.8 / 2	TRI	TRI		
SA_RCVENIN#	I SSTL1.8 / 2	IN	IN		
SA_RCVENOUT#	O SSTL1.8 / 2	HV	HV		

2.9.4 DDR / DDR2 SDRAM Channel B Interface

Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3	PU/PD
SB_DQ[63:0]	I/O SSTL1.8 / 2	TRI	TRI		
SB_DM[7:0]	O SSTL1.8 / 2	TRI	TRI		
SB_DQS[7:0]	I/O SSTL1.8 / 2	TRI	TRI		
SB_DQS[7:0]#	I/O SSTL1.8	TRI	TRI		
SB_MA[13:0]	O SSTL1.8 / 2	TRI	TRI		
SB_BS[2:0]	O SSTL1.8 / 2	TRI	TRI		
SB_RAS#	O SSTL1.8 / 2	TRI	TRI		
SB_CAS#	O SSTL1.8 / 2	TRI	TRI		
SB_WE#	O SSTL1.8 / 2	TRI	TRI		
SB_RCVENIN#	I SSTL1.8 / 2	IN	IN		
SB_RCVENOUT#	O SSTL1.8 / 2	HV	HV		

2.9.5 DDR / DDR2 Common Signals

Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3	PU/PD
SM_CK[1:0], SM_CK[4:3]	O SSTL1.8 / 2	TRI	TRI		
SM_CK[1:0]#, SM_CK[4:3]#	O SSTL1.8 / 2	TRI	TRI		
SM_CS[3:0]#	O SSTL1.8 / 2	TRI	TRI		
SM_CKE[3:0]	O SSTL1.8 / 2	LV	LV		
SM_ODT[3:0]	O SSTL1.8	0	LV		

2.9.6 DDR SDRAM Reference and Compensation

Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3	PU/PD
SMRCOMPN	I/O A	TRI	TRI after RCOMP		
SMRCOMPP	I/O A	TRI	TRI after RCOMP		
SMXSLEWIN	I A	IN	IN		
SMXSLEWOUT	O A	TRI	TRI after RCOMP		
SMYSLEWIN	I A	IN	IN		
SMYSLEWOUT	O A	TRI	TRI after RCOMP		
SMVREF[1:0]	I A	IN	IN		
SMOCDCOMP[1:0]	I A	TRI	TRI		

2.9.7 PCI Express Based Graphics Interface Signals

Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3	PU/PD
EXP_RXN[15:0]	I PCIE	TRI	TRI		
EXP_RXP[15:0]	I PCIE	TRI	TRI		
EXP_TXN[15:0]	O PCIE	TRI	TRI		
EXP_TXP[15:0]	O PCIE	TRI	TRI		
EXP_ICOMPO	I A	TRI	TRI		
EXP_COMPI	I A	TRI	TRI		

2.9.8 DMI

Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3	PU/PD
DMI_RXN[3:0]	I PCIE	TRI	TRI		
DMI_RXP[3:0]	I PCIE	TRI	TRI		
DMI_TXN[3:0]	O PCIE	TRI	TRI		
DMI_TXP[3:0]	O PCIE	TRI	TRI		

2.9.9 CRT DAC SIGNALS

Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3	PU/PD
RED	O A	LV			
RED#	O A	LV			
GREEN	O A	LV			
GREEN#	O A	LV			
BLUE	O A	LV			
BLUE#	O A	LV			
REFSET	O A	TRI	0.5 x Bandgap		255 ohm 1% resistor to ground
HSYNC	O HVCMOS	LV			
VSYNC	O HVCMOS	LV			

2.9.10 Analog TV-out Signals

Note: These signals are not supported on the Intel 915GME and Intel 910GMLE chipsets.

Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3	PU/PD
TVDAC_A	O A				
TVDAC_B	O A				
TVDAC_C	O A				
TV_IRTNA	O A				
TV_IRTNB	O A				
TV_IRTNC	O A				
TV_REFSET	O A				

2.9.11 LVDS Signals

Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3	PU/PD
LDVS Channel A					
LADATAP[2:0]	I/O LVDS	Drive VSS	Drive VSS		
LADATAN[2:0]	I/O LVDS	Drive VSS	Drive VSS		
LACLKP	I/O LVDS	Drive VSS	Drive VSS		
LACLKN	I/O LVDS	Drive VSS	Drive VSS		
LDVS Channel B					
LBDATAP[2:0]	I/O LVDS	Drive VSS	Drive VSS		
LBDATAN[2:0]	I/O LVDS	Drive VSS	Drive VSS		
LBCLKP	I/O LVDS	Drive VSS	Drive VSS		
LBCLKN	I/O LVDS	Drive VSS	Drive VSS		
LFP Panel control signal					
LVDD_EN	O HVCMOS	TRI	TRI		
LBKLT_EN	O HVCMOS	TRI	TRI		
LBKLT_CRTL	O HVCMOS	TRI	TRI		
LVDS Reference signal					
LVREFH	I Ref	IN	IN		
LVREFL	I Ref	IN	IN		

2.9.12 Display Data Channel (DDC) and GMBUS Support

Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3	PU/PD
LCTLA_CLK	I/O COD	PU	PU		
LCTLB_DATA	I/O COD	PU	PU		
DDCCLK	I/O COD	PU	PU		
DDCDATA	I/O COD	PU	PU		
LDDC_CLK	I/O COD	PU	PU		
LDDC_DATA	I/O COD	PU	PU		
SDVOCTRL_CLK	I/O COD	PU	PU		
SDVOCTRL_DATA	I/O COD	STRAP	PU		

2.9.13 PLL Signals

Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3	PU/PD
HCLKP	I Diff Clk	IN	IN		
HCLKN	I Diff Clk	IN	IN		
GCLKP	I Diff Clk	IN	IN		
GCLKN	I Diff Clk	IN	IN		
DREF_CLKP	I Diff Clk	IN	IN		
DREF_CLKN	I Diff Clk	IN	IN		
DREF_SSCLKP	I Diff Clk	IN	IN		
DREF_SSCLKN	I Diff Clk	IN	IN		

2.9.14 Reset and Miscellaneous Signals

Signal Name	Type	State during RSTIN# Assertion	State after RSTIN# Deassertion	S3	PU/PD
RSTIN#	I HVCMOS	IN	IN		
PWROK	I HVCMOS	HV	HV		
H_BSEL [2:0] (CFG[2:0])	I HVCMOS				
CFG[17:3]	I AGTL+				
CFG[20:18]	I HVCMOS				
BM_BUSY#	O HVCMOS	HV STRAP	HV		
THRMTRIP#	O COD				
EXT_TS[1:0]#	I HVCMOS	IN	IN		

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3 GMCH Register Description

Table 3-1 shows the register-related terminology that is used.

Table 3-1. Register Terminology

RO	Read Only bit(s). Writes to these bits have no effect.
RS/WC	Read Set / Write Clear bit(s). These bits are set to 1 when read and then will continue to remain set until written. A write of 1 clears (sets to 0) the corresponding bit(s) and a write of 0 has no effect.
R/W	Read / Write bit(s). These bits can be read and written.
R/WC	Read / Write Clear bit(s). These bits can be read. Internal events may set this bit. A write of 1 clears (sets to 0) the corresponding bit(s) and a write of 0 has no effect.
R/WC/S	Read / Write Clear / Sticky bit(s). These bits can be read. Internal events may set this bit. A write of 1 clears (sets to 0) the corresponding bit(s) and a write of 0 has no effect. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express* related bits a cold reset is “Power Good Reset” as defined in the PCI Express spec).
R/W/L	Read / Write / Lockable bit(s). These bits can be read and written. Additionally there is a bit (which may or may not be a bit marked R/W/L) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).
R/W/S	Read / Write / Sticky bit(s). These bits can be read and written. Bits are not cleared by "warm" reset, but will be reset with a cold/complete reset (for PCI Express related bits a cold reset is “Power Good Reset” as defined in the PCI Express spec).
R/WSC	Read / Write Self Clear bit(s). These bits can be read and written. When the bit is 1, hardware may clear the bit to 0, based upon internal events, possibly sooner than any subsequent read could retrieve a 1.
R/WSC/L	Read / Write Self Clear / Lockable bit(s). These bits can be read and written. When the bit is 1, hardware may clear the bit to 0, based upon internal events, possibly sooner than any subsequent read could retrieve a 1. Additionally there is a bit (which may or may not be a bit marked R/W/L) that, when set, prohibits this bit field from being writeable (bit field becomes Read Only).
R/WC	Read Write Clear bit(s). These bits can be read and written. However, a write of 1 clears (sets to 0) the corresponding bit(s) and a write of 0 has no effect.
R/WO	Write Once bit(s). Once written, bits with this attribute become Read Only. These bits can only be cleared by a Reset.
W	Write Only. Whose bits may be written, but will always-return 0’s when read. They are used for write side effects. Any data written to these registers cannot be retrieved.

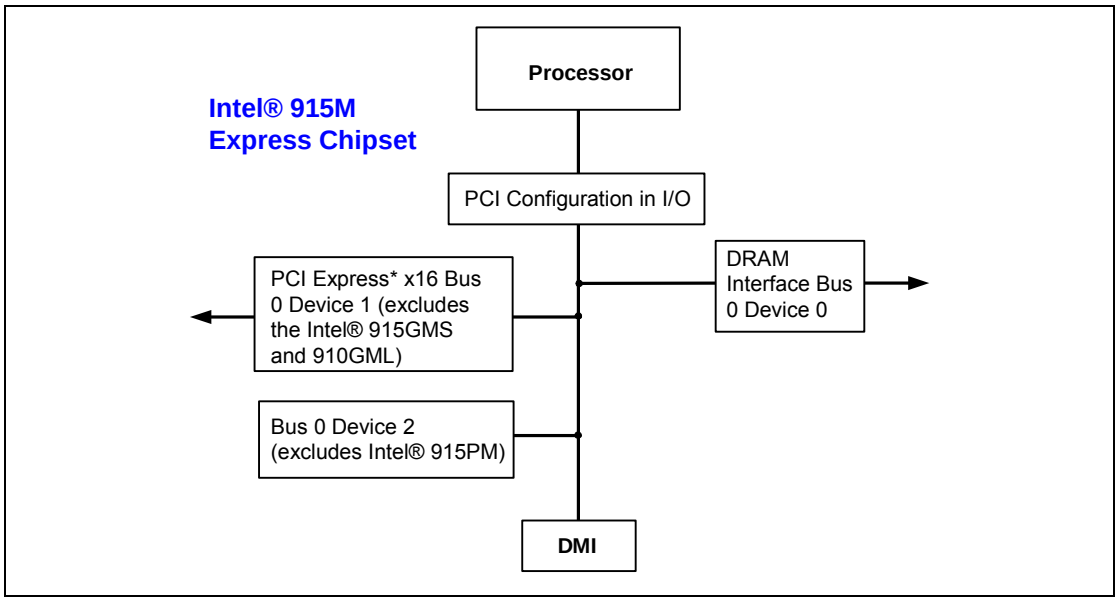
3.1 Configuration Process and Registers

3.1.1 Platform Configuration Structure

In platforms that support DMI (e.g., this GMCH) the configuration structure is significantly different from previous Hub architectures. The DMI physically connects the GMCH and the ICH6; so, from a configuration standpoint, the DMI is logically PCI bus 0. As a result, all devices internal to the GMCH and the ICH6 appear to be on PCI bus 0. The system's primary PCI expansion bus is physically attached to the ICH6 and, from a configuration perspective, appears to be a hierarchical PCI bus behind a PCI-to-PCI bridge and therefore has a programmable PCI bus number. The PCI Express Graphics Attach appears to system software to be a real PCI bus behind a PCI-to-PCI bridge that is a device resident on PCI bus 0.

Note: That a physical PCI bus 0 does not exist and that DMI and the internal devices in the GMCH and ICH6 logically constitute PCI Bus 0 to configuration software. This is shown in the following figure.

Figure 3-1. Conceptual Platform PCI Configuration Diagram



The GMCH contains three PCI devices within a single physical component. The configuration registers for the three devices are mapped as devices residing on PCI bus 0.

- **Device 0:** Host Bridge/DRAM Controller. Logically this appears as a PCI device residing on PCI bus 0. Device 0 contains the standard PCI header registers, PCI Express base address register, DRAM control (including thermal/throttling control), and other GMCH specific registers.
- **Device 1:** Host-PCI Express Bridge. Logically this appears as a "virtual" PCI-to-PCI bridge residing on PCI bus 0 and is compliant with PCI Express Specification rev 1.0. Device 1 contains the standard PCI-to-PCI bridge registers and the standard PCI Express/PCI configuration registers (including the PCI Express memory address mapping). It also contains Isochronous and Virtual Channel controls in the PCI Express extended configuration space.
- **Device 2:** Internal Graphics Control. Logically, this appears as a PCI device residing on PCI bus 0. Physically, device 2 contains the configuration registers for 3D, 2D, and display functions.



Table 3-2. Device Number Assignment for Internal GMCH Devices

GMCH Function	Device#
Host Bridge / DRAM Controller	Device 0
Host-to-PCI Express* Bridge (virtual PCI-to-PCI)	Device 1
Internal Graphics Control	Device 2

3.1.2 General Routing Configuration Accesses

The GMCH supports two PCI related interfaces: DMI and PCI Express. PCI and PCI Express configuration cycles are selectively routed to one of these interfaces. The GMCH is responsible for routing configuration cycles to the proper interface. Configuration cycles to the ICH6 internal devices and Primary PCI (including downstream devices) are routed to the ICH6 via DMI. Configuration cycles to both the PCI Express Graphics PCI compatibility configuration space and the PCI Express Graphics extended configuration space are routed to the PCI Express Graphics port.

A detailed description of the mechanism for translating CPU I/O bus cycles to configuration cycles is described below.

3.1.3 Standard PCI Bus Configuration Mechanism

The PCI bus defines a slot based configuration space that allows each device to contain up to eight functions with each function containing up to 256, 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space: Configuration Read and Configuration Write. Memory and I/O spaces are supported directly by the CPU. Configuration space is supported by a mapping mechanism implemented within the GMCH.

The configuration access mechanism makes use of the CONFIG_ADDRESS Register (at I/O address 0CF8h though 0CFBh) and CONFIG_DATA Register (at I/O address 0CFCh though 0CFFh). To reference a configuration register a DW I/O write cycle is used to place a value into CONFIG_ADDRESS that specifies the PCI bus, the device on that bus, the function within the device and a specific configuration register of the device function being accessed. CONFIG_ADDRESS [31] must be 1 to enable a configuration cycle. CONFIG_DATA then becomes a window into the four bytes of configuration space specified by the contents of CONFIG_ADDRESS. Any read or write to CONFIG_DATA will result in the GMCH translating the CONFIG_ADDRESS into the appropriate configuration cycle.

The GMCH is responsible for translating and routing the CPU's I/O accesses to the CONFIG_ADDRESS and CONFIG_DATA registers to internal GMCH configuration registers, DMI or PCI Express.

3.1.4 Logical PCI Bus 0 Configuration Mechanism

The GMCH decodes the Bus Number (bits 23:16) and the Device Number fields of the CONFIG_ADDRESS register. If the Bus Number field of CONFIG_ADDRESS is 0 the configuration cycle is targeting a PCI Bus 0 device. The Host-DMI Bridge entity within the GMCH is hardwired as Device 0 on PCI Bus 0. The Host-PCI Express Bridge entity within the GMCH is hardwired as Device 1 on PCI Bus 0. Device 2 contains the control registers for the Integrated Graphics Controller. The ICH6 decodes the Type 0 access and generates a configuration access to the selected internal device.

3.1.5 Primary PCI and Downstream Configuration Mechanism

If the Bus Number in the CONFIG_ADDRESS is non-zero, and falls outside the range claimed by the Host-PCI Express bridge (not between lower bound in device's SUBORDINATE BUS NUMBER register and upper bound in device's SECONDARY BUS NUMBER register), the GMCH would generate a Type 1 DMI Configuration Cycle. This DMI configuration cycle will be sent over the DMI.

If the cycle is forwarded to the ICH6 via the DMI, the ICH6 compares the non-zero Bus Number with the SECONDARY BUS NUMBER and SUBORDINATE BUS NUMBER registers of its PCI-to-PCI bridges to determine if the configuration cycle is meant for Primary PCI, one of the ICH's devices, the DMI, or a downstream PCI bus.

Figure 3-2. DMI Type 0 Configuration Address Translation

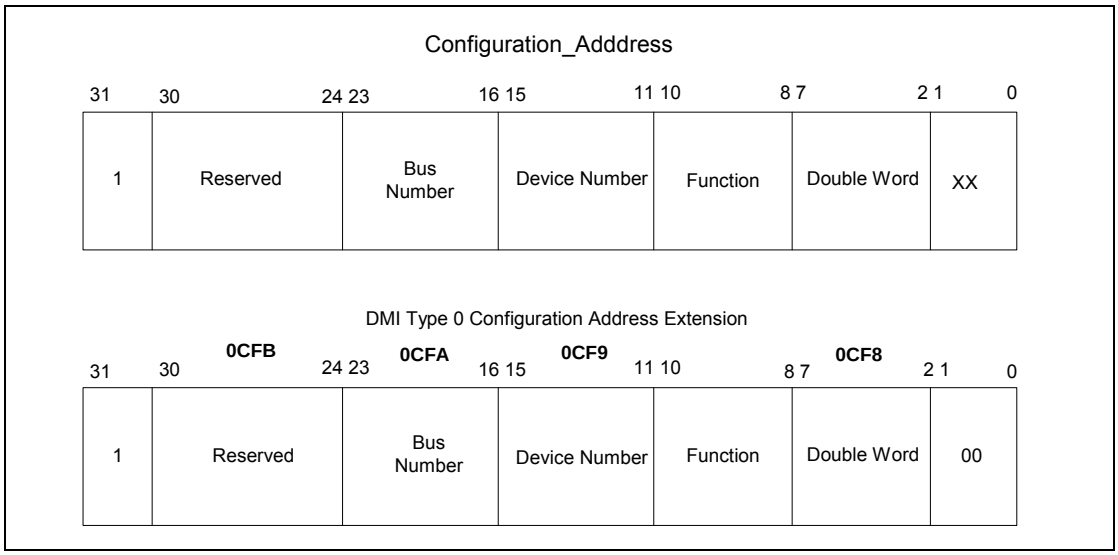
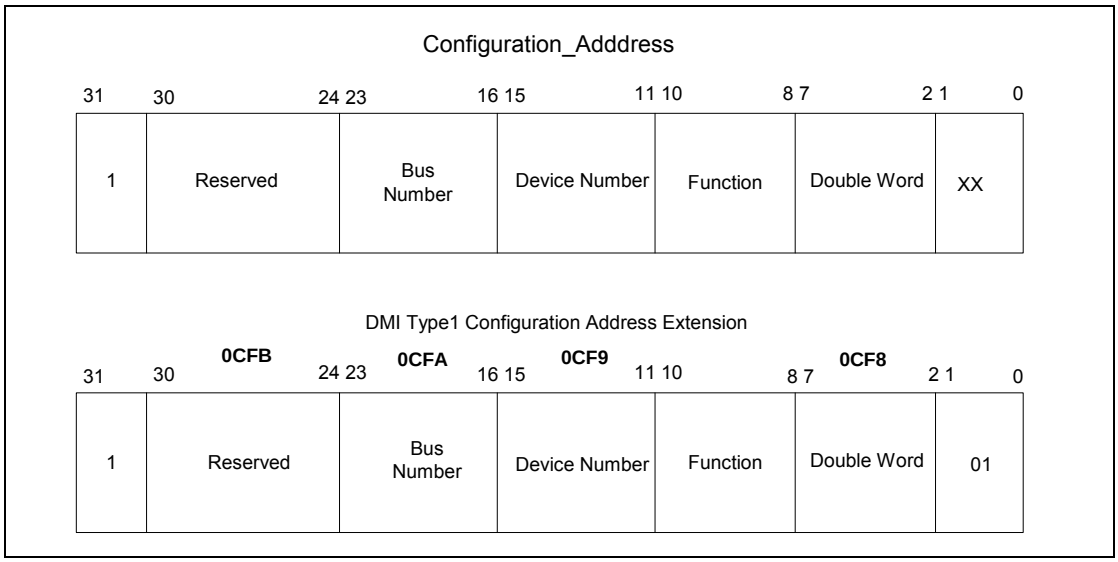


Figure 3-3. DMI Type 1 Configuration Address Translation



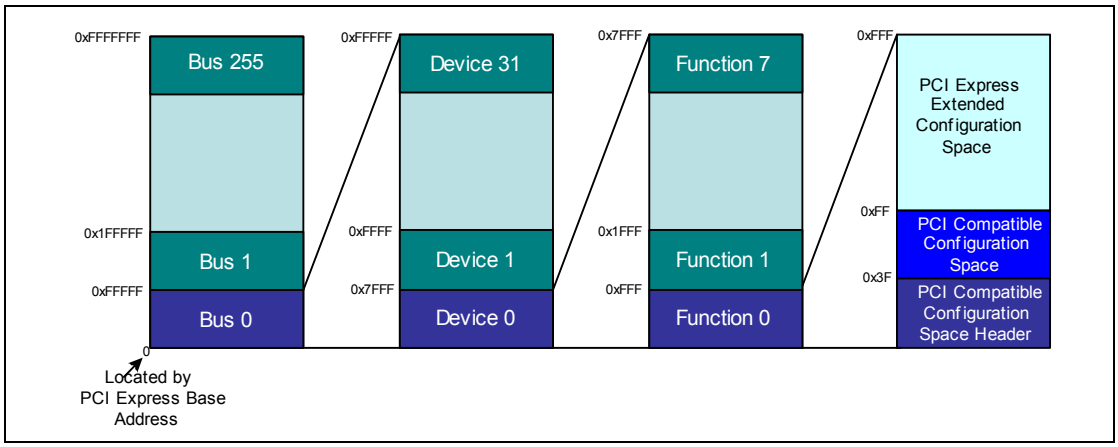
3.1.6 PCI Express Enhanced Configuration Mechanism

PCI Express extends the configuration space to 4096 bytes per device/function as compared to 256 bytes allowed by PCI Specification Revision 2.3. PCI Express configuration space is divided into a PCI 2.3 compatible region, which consists of the first 256 bytes of a logical device's configuration space and a PCI Express extended region, which consists of the remaining configuration space.

The PCI compatible region can be accessed using either the mechanism defined in the previous section or using the enhanced PCI Express configuration access mechanism described in this section. The extended configuration registers may only be accessed using the enhanced PCI Express configuration access mechanism. To maintain compatibility with PCI configuration addressing mechanisms, system software must access the extended configuration space using 32-bit operations (32-bit aligned) only. These 32-bit operations include byte enables allowing only appropriate bytes within the DWORD to be accessed. Locked transactions to the PCI Express memory mapped configuration address space are not supported. All changes made using either access mechanism are equivalent.

The enhanced PCI Express configuration access mechanism utilizes a flat memory-mapped address space to access device configuration registers. This address space is reported by the system firmware to the operating system. PCIEXBAR defines the base address for the 256-MB block of addresses below the top of addressable memory (currently 4 GB) for the configuration space associated with all devices and functions that are potentially a part of the PCI Express root complex hierarchy. The PCI Express Configuration Transaction Header includes an additional 4 bits (Extended Register Address[3:0]) between the Function Number and Register Address fields to provide indexing into the 4 KB of configuration space allocated to each potential device. For PCI Compatible Configuration Requests, the Extended Register Address field must be all 0's.

Figure 3-4. Memory Map to PCI Express Device Configuration Space



Just the same as with PCI devices, each device is selected based on decoded address information that is provided as a part of the address portion of Configuration Request packets. A PCI Express device will decode all address information fields (bus, device, function and extended address numbers) to provide access to the correct register.

To access this space (steps 1, 2, 3 are done only once by BIOS),

1. Use the PCI compatible configuration mechanism to enable the PCI Express enhanced configuration mechanism by writing 1 to bit 31 of the DEVEN register.
2. Use the PCI compatible configuration mechanism to write an appropriate PCI Express base address into the PCIEXBAR register.
3. Calculate the host address of the register you wish to set using (PCI Express base + (bus number * 1 MB) + (device number * 32 kB) + (function number * 4 kB) + (1 B * offset within the function) = host address).
4. Use a memory write or memory read cycle to the calculated host address to write to or read from that register.

31 28	27 20	19 15	14 12	11 8	7 2	1	0
Base	Bus	Device	Func.	Extended	Register Number	x	x

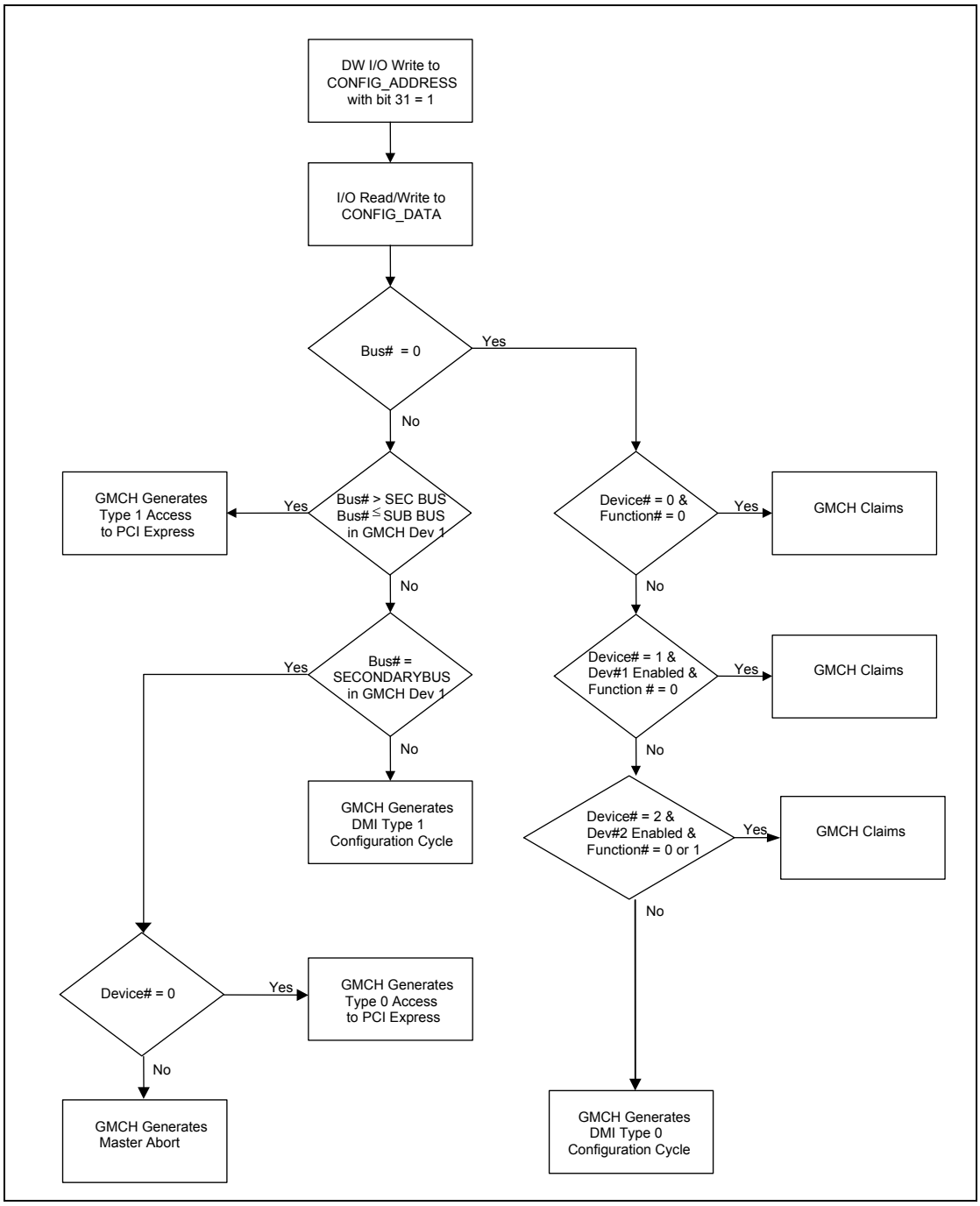
PCI Express Configuration Writes:

- Internally the host interface unit will translate writes to PCI Express extended configuration space to configurations on the backbone.
- Writes to extended space are posted on the FSB, but non-posted on the PEG or DMI pins (i.e., translated to config writes).

See the PCI Express specification for more information on both the PCI 2.3 compatible and PCI Express enhanced configuration mechanism and transaction rules.

3.1.7 GMCH Configuration Cycle Flow Chart

Figure 3-5. GMCH Configuration Cycle Flow Chart



3.2 I/O Mapped Registers

The GMCH contains two registers that reside in the CPU I/O address space – the Configuration Address (CONFIG_ADDRESS) Register and the Configuration Data (CONFIG_DATA) Register. The Configuration Address Register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

3.2.1 CONFIG_ADDRESS—Configuration Address Register

I/O Address: 0CF8h Accessed as a DW
Size: 32 bits

CONFIG_ADDRESS is a 32 bit register that can be accessed only as a DW. A Byte or Word reference will "pass through" the Configuration Address Register and DMI onto the PCI_A bus as an I/O cycle. The CONFIG_ADDRESS register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Bit	Access & Default	Description
31	R/W 0b	**Configuration Enable (CFGE) -** When this bit is set to 1, accesses to PCI configuration space are enabled. If this bit is reset to 0, accesses to PCI configuration space are disabled.
30:24	RO 00h	**Reserved**
23:16	R/W 00h	**Bus Number -** If the Bus Number is programmed to 00h the target of the Configuration Cycle is a PCI Bus #0 agent. If this is the case and the GMCH is not the target (i.e. the device number is >= 3 and not equal to 7), then a DMI Type 0 Configuration Cycle is generated. If the Bus Number is non-zero, and does not fall within the ranges enumerated by device #1's SECONDARY BUS NUMBER or SUBORDINATE BUS NUMBER Register, then a DMI Type 1 Configuration Cycle is generated. If the Bus Number is non-zero and matches the value programmed into the SECONDARY BUS NUMBER Register of device #1, a Type 0 PCI configuration cycle will be generated on PCI Express Graphics. If the Bus Number is non-zero, greater than the value in the SECONDARY BUS NUMBER register of device #1 and less than or equal to the value programmed into the SUBORDINATE BUS NUMBER Register of device #1 a Type 1 PCI configuration cycle will be generated on PCI Express Graphics. This field is mapped to byte 8 [7:0] of the request header format during PCI Express Configuration cycles and A[23:16] during the DMI Type 1 configuration cycles.
15:11	R/W 00h	**Device Number -** This field selects one agent on the PCI bus selected by the Bus Number. When the Bus Number field is "00" the GMCH decodes the Device Number field. The GMCH is always Device Number 0 for the Host bridge entity, Device Number 1 for the Host-PCI Express entity. Therefore, when the Bus Number =0 and the Device Number equals 0,1, 2 or 7 the internal GMCH devices are selected. This field is mapped to byte 6 [7:3] of the request header format during PCI Express and DMI Configuration cycles.
10:8	R/W 000b	**Function Number** This field allows the configuration registers of a particular function in a multi-function device to be accessed. The GMCH ignores configuration cycles to it's internal Devices if the function number is not equal to 0 or 1. This field is mapped to byte 6 [2:0] of the request header format during PCI Express and DMI Configuration cycles.

Bit	Access & Default	Description
7:2	R/W 00h	**Register Number** This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address Register. This field is mapped to byte 7 [7:2] of the request header format for during PCI Express and DMI Configuration cycles.
1:0	RO 00b	**Reserved**

3.2.2 CONFIG_DATA—Configuration Data Register

I/O Address: 0CFCh
Size: 32 bits

CONFIG_DATA is a 32-bit read/write window into configuration space. The portion of configuration space that is referenced by CONFIG_DATA is determined by the contents of CONFIG_ADDRESS.

Bit	Access & Default	Description
31:0	R/W 0000 0000 h	**Configuration Data Window (CDW)** If bit 31 of CONFIG_ADDRESS is 1, any I/O access to the CONFIG_DATA register will produce a configuration transaction using the contents of CONFIG_ADDRESS to determine the bus, device, function, and offset of the register to be accessed.

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4 Host Bridge Device 0 - Configuration Registers (D0:F0)

Warning: Address locations that are not listed are considered Reserved registers locations. Reads to Reserved registers may return non-zero values. Writes to reserved locations may cause system failures.

4.1 Host Bridge Device 0 Configuration Register Space

All registers that are defined in the PCI 2.3 specification, but are not necessary or implemented in this component are simply not included in this document. The reserved/unimplemented space in the PCI configuration header space is not documented as such in this summary.

Address Offset	Register Symbol	Register Name	Default Value	Access
00-01h	VID	Vendor Identification	8086h	RO
02-03h	DID	Device Identification	2590h	RO
04-05h	PCICMD	PCI Command	0006h	RO, R/W
06-07h	PCISTS	PCI Status	0090h	RO, R/WC
08h	RID	Revision Identification	00h See register description	RO
09-0Bh	CC	Class Code	060000h	RO
0Ch		***Reserved***		
0Dh	MLT	Master Latency Timer	00h	RO
0Eh	HDR	Header Type	00h	RO
0F-2Bh		***Reserved***		
2C-2Dh	SVID	Subsystem Vendor Identification	0000h	R/WO
2E-2Fh	SID	Subsystem Identification	0000h	R/WO
30-33h		***Reserved***		
34-34h	CAPPTR	Capabilities Pointer	E0h	RO
35-3Fh		***Reserved***		
40-43h	EPBAR	EP Root Complex MMIO Base Address	00000000h	RO, R/W
44-47h	MCHBAR	MCH MMIO Base Address	00000000h	RO, R/W
48-4Bh	PCIEXBAR	PCI Express MMIO Base Address	E0000000h	RO, R/W
4C-4Fh	DMIBAR	DMI Root Complex MMIO Base Address	00000000h	RO, R/W
50-51h		***Reserved***		
52-53h	GGC	Graphics Control Register 82915GM/GML/GMS only	0030h	RO, R/W
54-57h	DEVEN	Device Enable	00000019h	RO, R/W, R/W/L
58-8Fh		***Reserved***		
90h	PAM0	Programmable Attribute Map 0	00h	RO, R/W
91h	PAM1	Programmable Attribute Map 1	00h	RO, R/W
92h	PAM2	Programmable Attribute Map 2	00h	RO, R/W
93h	PAM3	Programmable Attribute Map 3	00h	RO, R/W

94h	PAM4	Programmable Attribute Map 4	00h	RO, R/W
95h	PAM5	Programmable Attribute Map 5	00h	RO, R/W
96h	PAM6	Programmable Attribute Map 6	00h	RO, R/W
97h	LAC	Legacy Access Control	00h	RO, R/W
98-9Bh		***Reserved***		
9Ch	TOLUD	Top of Low Used Dram	08h	RO, R/W
9Dh	SMRAM	System Management RAM Control	02h	RO, R/W/L
9Eh	ESMRAMC	Extended System Management RAM Control	38h	RO, R/W, R/WC, R/W/L
9F-C7h		***Reserved***		
C8-C9h	ERRSTS	Error Status	0000h	RO, R/W/C
CA-CBh	ERRCMD	Error Command	0000h	RO, R/W
CC-DFh		***Reserved***		
E0-E8h	CAPID0	Capability Identifier	xxxxxxxxxxxx90009h	RO
E9-FFh		***Reserved***		

4.1.1 VID—Vendor Identification

PCI Device: 0
Address Offset: 00h
Default Value: 8086h
Access: RO
Size: 16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access	Description
15:0	RO 8086h	**Vendor Identification Number (VID):** PCI standard identification for Intel.

4.1.2 DID—Device Identification

PCI Device: 0
Address Offset: 02h
Default Value: 2590h
Access: RO
Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 2590 h	**Device Identification Number (DID):** Identifier assigned to the GMCH core/primary PCI device.

4.1.3 PCICMD—PCI Command

PCI Device: 0
Address Offset: 04h
Default Value: 0006h

Access: RO, R/W
Size: 16 bits

GMCH Device #0 does not physically reside on PCI_A many of the bits are not implemented.

Bit	Access & Default	Description
15:10	RO 00h	**Reserved**
9	RO 0 b	**Fast Back-to-Back Enable (FB2B):** This bit controls whether or not the master can do fast back-to-back write. Since device 0 is strictly a target this bit is not implemented and is hardwired to 0. Writes to this bit position have no affect.
8	R/W 0 b	**SERR Enable (SERRE):** This bit is a global enable bit for Device 0 SERR messaging. The GMCH does not have an SERR signal. The GMCH communicates the SERR condition by sending an SERR message over GMCH ICH Serial Interface (DMI) to the ICH. If this bit is set to a 1, the GMCH is enabled to generate SERR messages over DMI for specific Device 0 error conditions that are individually enabled in the ERRCMD register. The error status is reported in the ERRSTS and PCISTS registers. If SERRE is clear, then the SERR message is not generated by the GMCH for Device 0. Note that this bit only controls SERR messaging for the Device 0. Device 1 has its own SERRE bits to control error reporting for error conditions occurring on their respective devices. The control bits are used in a logical OR manner to enable the SERR DMI message mechanism.
7	RO 0 b	**Address/Data Stepping Enable (ADSTEP):** Address/data stepping is not implemented in the GMCH, and this bit is hardwired to 0. Writes to this bit position have no effect.
6	RO 0 b	**Parity Error Enable (PERRE):** PERRB is not implemented by the GMCH and this bit is hardwired to 0. Writes to this bit position have no effect.
5	RO 0 b	**VGA Palette Snoop Enable (VGASNOOP):** The GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
4	RO 0 b	**Memory Write and Invalidate Enable (MWIE):** The GMCH will never issue memory write and invalidate commands. This bit is therefore hardwired to 0. Writes to this bit position will have no effect.
3	RO 0 b	**Special Cycle Enable (SCE):** The GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
2	RO 1 b	**Bus Master Enable (BME):** The GMCH is always enabled as a master on DMI. This bit is hardwired to a 1. Writes to this bit position have no effect.
1	RO 1 b	**Memory Access Enable (MAE):** The GMCH always allows access to main memory. This bit is not implemented and is hardwired to 1. Writes to this bit position have no effect.
0	RO 0 b	**I/O Access Enable (IOAE):** This bit is not implemented in the GMCH and is hardwired to a 0. Writes to this bit position have no effect.

4.1.4 PCISTS—PCI Status

PCI Device: 0

Address Offset: 06h
Default Value: 0090h
Access: RO, R/WC
Size: 16 bits

This status register reports the occurrence of error events on Device 0's PCI interface. Since the GMCH Device 0 does not physically reside on PCI_A many of the bits are not implemented.

Bit	Access & Default	Description
15	RO 0 b	**Detected Parity Error (DPE):** The GMCH does not implement this bit and it is hardwired to a 0. Writes to this bit position have no effect.
14	R/W/C 0 b	**Signaled System Error (SSE):** This bit is set to 1 when the GMCH Device 0 generates an SERR message over DMI for any enabled Device 0 error condition. Device 0 error conditions are enabled in the PCICMD and ERRCMD registers. Device 0 error flags are read/reset from the PCISTS or ERRSTS registers. Software clears this bit by writing a 1 to it.
13	R/W/C 0 b	**Received Unsupported Request (RURS):** This bit is set when the MCH generates a DMI request that receives a Unsupported request completion. Software clears this bit by writing a 1 to it.
12	R/W/C 0 b	**Received Completion Abort Status (RCAS):** This bit is set when the MCH generates a DMI request that receives a completion abort. Software clears this bit by writing a 1 to it. If ERRCMD bit 6 is set, an SERR special cycle is generated on the DMI.
11	RO 0 b	**Signaled Target Abort Status (STAS):** The GMCH will not generate a Target Abort DMI completion packet or Special Cycle. This bit is not implemented in the GMCH and is hardwired to a 0. Writes to this bit position have no effect.
10:9	RO 00 b	**DEVSEL Timing (DEVT):** These bits are hardwired to "00". Writes to these bit positions have no affect. Device 0 does not physically connect to PCI_A. These bits are set to "00" (fast decode) so that optimum DEVSEL timing for PCI_A is not limited by the GMCH.
8	RO 0 b	**Master Data Parity Error Detected (DPD):** PERR signaling and messaging are not implemented by the GMCH therefore this bit is hardwired to 0. Writes to this bit position have no effect.
7	RO 1 b	**Fast Back-to-Back (FB2B):** This bit is hardwired to 1. Writes to these bit positions have no effect. Device 0 does not physically connect to PCI_A. This bit is set to 1 (indicating fast back-to-back capability) so that the optimum setting for PCI_A is not limited by the GMCH.
6:5	RO 00 b	**Reserved**
4	RO 1 b	**Capability List (CLIST):** This bit is hardwired to 1 to indicate to the configuration software that this device/function implements a list of new capabilities. A list of new capabilities is accessed via register CAPPTR at configuration address offset 34h. Register CAPPTR contains an offset pointing to the start address within configuration space of this device where the Capability standard register resides.
3:0	RO 0 h	**Reserved**

4.1.5 RID—Revision Identification

PCI Device: 0

Address Offset: 08h
Default Value: xxh
Access: RO
Size: 8 bits

This register contains the revision number of the GMCH Device #0.

Bit	Access & Default	Description
7:0	RO 00 h	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the GMCH Device 0..

4.1.6 CC—Class Code

PCI Device: 0
Address Offset: 09h
Default Value: 060000h
Access: RO
Size: 24 bits

This register identifies the basic function of the device, a more specific sub-class, and a register-specific programming interface.

Bit	Access & Default	Description
23:16	RO 06 h	**Base Class Code (BCC) –** This is an 8-bit value that indicates the base class code for the GMCH. This code has the value 06h, indicating a Bridge device.
15:8	RO 00 h	**Sub-Class Code (SUBCC) –** This is an 8-bit value that indicates the category of Bridge into which the GMCH falls. The code is 00h indicating a Host Bridge.
7:0	RO 00 h	**Programming Interface (PI) –** This is an 8-bit value that indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

4.1.7 MLT—Master Latency Timer

PCI Device: 0
Address Offset: 0Dh
Default Value: 00h
Access: RO
Size: 8 bits

Device #0 in the GMCH is not a PCI master. Therefore this register is not implemented.

Bit	Access & Default	Description
7:0	RO 00 h	**Reserved.**

4.1.8 HDR—Header Type

PCI Device: 0
Address Offset: 0Eh
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Access & Default	Description
7:0	RO 00 h	**PCI Header (HDR):** This field always returns 0 to indicate that the GMCH is a single function device with standard header layout. Reads and writes to this location have no effect.

4.1.9 SVID—Subsystem Vendor Identification

PCI Device: 0
Address Offset: 2Ch
Default Value: 0000h
Access: R/WO
Size: 16 bits

This value is used to identify the vendor of the subsystem.

Bit	Access & Default	Description
15:0	R/WO 0000 h	**Subsystem Vendor ID (SUBVID):** This field should be programmed during boot-up to indicate the vendor of the system board. After it has been written once, it becomes read only.



4.1.10 SID—Subsystem Identification

PCI Device: 0
Address Offset: 2Eh
Default Value: 0000h
Access: R/WO
Size: 16 bits

This value is used to identify a particular subsystem.

Bit	Access & Default	Description
15:0	R/WO 0000 h	**Subsystem ID (SUBID)**: This field should be programmed during BIOS initialization. After it has been written once, it becomes read only.

4.1.11 CAPPTR—Capabilities Pointer

PCI Device: 0
Address Offset: 34h
Default Value: E0h
Access: RO
Size: 8 bits

The CAPPTR provides the offset that is the pointer to the location of the first device capability in the capability list.

Bit	Access & Default	Description
7:0	RO E0 h	**Pointer to the offset of the first capability ID register block:** In this case the first capability is the product-specific Capability Identifier (CAPID0).

4.1.12 EPBAR—Egress Port Base Address

PCI Device: 0
Address Offset: 40h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

This is the base address for the Egress Port Root Complex MMIO configuration space. This window of addresses contains the Egress Port Root Complex Register set for the PCI Express Hierarchy associated with the GMCH. There is no physical memory within this 4-kB window that can be addressed. The 4 kB reserved by this register does not alias to any PCI2.3 compliant memory mapped space.

On reset, this register is disabled and must be enabled by writing a 1 to RCBAREN [Dev 0, offset 54h, bit 27]

Bit	Access & Default	Description
31:12	R/W 0000 0 h	**Egress Port RCRB Base Address –** This field corresponds to bits 31 to 12 of the base address Egress port RCRB MMIO configuration space. BIOS will program this register resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within total addressable memory space of 4GB. System Software uses this base address to program the Egress Port RCRB and associated registers.
11:0		**Reserved**



4.1.13 MCHBAR—GMCH Register Range Base Address

PCI Device: 0
Address Offset: 44h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

This is the base address for the GMCH MMIO Configuration space. There is no physical memory within this 16-kB window that can be addressed. The 16KB reserved by this register does not alias to any PCI2.3 compliant memory mapped space.

On reset, this register is disabled and must be enabled by writing a 1 to MCHBAREN [Dev 0, offset 54h, bit 28].

Bit	Access & Default	Description
31:14	R/W 0000 h	**MCHBAR Base Address** – This field corresponds to bits 31 to 14 of the base address MCHBAR configuration space. BIOS will program this register resulting in a base address for a 16-kB block of contiguous memory address space. This register ensures that a naturally aligned 16KB space is allocated within total addressable memory space of 4 GB. System Software uses this base address to program the GMCH register set.
13:0		Reserved

4.1.14 PCIEXBAR—PCI Express Register Range Base Address

PCI Device: 0
Address Offset: 48h
Default Value: E0000000h
Access: RO, R/W
Size: 32 bits

This is the base address for the PCI Express configuration space. This window of addresses contains the 4 kB of configuration space for each PCI Express device that can potentially be part of the PCI Express Hierarchy associated with the GMCH. There is no actual physical memory within this 256-MB window that can be addressed. Each PCI Express Hierarchies requires a PCI Express BASE register. The GMCH supports one PCI Express hierarchy.

The 256 MB reserved by this register does not alias to any PCI2.3 compliant memory mapped space. For example, MCHBAR reserves a 16-KB space and reserves a 4-KB space both outside of PCIEXBAR space. They cannot be overlaid on the space reserved by PCIEXBAR for Device 0.

On reset, this register is disabled and must be enabled by writing a 1 to PCIEXBAREN [Dev 0, offset 54h, bit 31]

If the PCI Express Base address [bits 31:28] were set to Fh, an overlap with the High BIOS area, APIC ranges would result. Software must guarantee that these ranges do not overlap. The PCI Express Base Address cannot be less than the maximum address written to the TOP of physical memory register (TOLUD).

Bit	Access & Default	Description
31:28	R/W 1110 b	PCI Express Base Address – This field corresponds to bits 31 to 28 of the base address for PCI Express enhanced configuration space. BIOS will program this register resulting in a base address for a 256 MB block of contiguous memory address space. Having control of those particular 4 bits insures that this base address will be on a 256-MB boundary, above the lowest 256 MB and still within total addressable memory space, currently 4 GB. Configuration software will read this register to determine where the 256 MB range of addresses resides for this particular host bridge. The address used to access the PCI Express configuration space for a specific device can be determined as follows: *PCI Express Base Address + Bus Number * 1MB + Device Number * 32 kB + Function Number * 4 kB* The address used to access the PCI Express configuration space for Device 1 in this component would be as follows. *PCI Express Base Address + 0 * 1 MB + 1 * 32 kB + 0 * 4 kB = PCI Express Base Address + 32 kB.* NOTE: This address is at the beginning of the 4 kB space that contains both the PCI compatible configuration space and the PCI Express extended configuration space.
27:0		**Reserved**

4.1.15 DMIBAR—DMI Root Complex Register Range Base Address

PCI Device: 0
Address Offset: 4Ch
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

This is the base address for the DMI Root Complex MMIO configuration space. This window of addresses contains the DMI Root Complex Register set for the PCI Express Hierarchy associated with the GMCH. There is no physical memory within this 4KB window that can be addressed. The 4 kB reserved by this register does not alias to any PCI2.3 compliant memory mapped space.

On reset, this register is disabled and must be enabled by writing a 1 to RCBAREN [Dev 0, offset 54h, and bit 29].

Bit	Access & Default	Description
31:12	R/W 0000 0 h	**DMI root complex MMIO register set Base Address –** This field corresponds to bits 31 to 12 of the base address DMI RCRB MMIO configuration space. BIOS will program this register resulting in a base address for a 4KB block of contiguous memory address space. This register ensures that a naturally aligned 4KB space is allocated within total addressable memory space of 4GB. System Software uses this base address to program the DMI RCRB registers.
11:0		**Reserved**

4.1.16 GGC-GMCH Graphics Control Register (Device 0)

PCI Device: 0
Address Offset: 52-53h
Default Value: 0030h
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Descriptions
15:7		**Reserved**
6:4	R/W 011 b	**Graphics Mode Select (GMS).** This field is used to select the amount of Main Memory that is pre-allocated to support the Internal Graphics device in VGA (non-linear) and Native (linear) modes. *Stolen Memory Bases is located between (TOLUD – SMSize) to TOUD.* 000 = No memory pre-allocated. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80. 001 = DVMT (UMA) mode, 1 MB of memory pre-allocated for frame buffer. 010 = Reserved 011 = DVMT (UMA) mode, 8 MB of memory pre-allocated for frame buffer. 100 : 111 = Reserved Note: This register is locked and becomes Read Only when the D_LCK bit in the SMRAM register is set. If IGD is disabled, this field should be set to 000b
3:2		**Reserved**
1	R/W/L 0 b	**IGD VGA Disable (IVD).** **0:** Enable **(Default).** Device 2 (IGD) claims VGA memory and IO cycles, the Sub-Class Code within Device 2 Class Code register is 00. **1:** Disable. Device 2 (IGD) does not claim VGA cycles (Mem and IO), and the Sub-Class Code field within Device 2 function 0 Class Code register is 80.
0		**Reserved**

4.1.17 DEVEN—Device Enable

PCI Device: 0
Address Offset: 54h
Default Value: 00000019h
Access: RO, R/W, R/W/L
Size: 32 bits

This register allows for enabling/disabling of PCI devices and functions that are within the GMCH. This table describes the behavior of all combinations of transactions to devices controlled by this register.

Bit	Access & Default	Description
31	R/W 0 b	**82915GM / 82915GME / 82915PM GMCH:** **PCIEXBAR Enable (PCIEXBAREN):** 0: The PCIEXBAR register is disabled. Memory read and write transactions proceed as if there were no PCIEXBAR register. 1: The PCIEXBAR register is enabled. Memory read and write transactions whose address bits 31:28 match PCIEXBAR 31:28 will be translated to configuration reads and writes within the GMCH. **82910GML / 82910GMLE / 82915GMS:** Reserved
30		**Reserved**
29	R/W/L 0 b	**DMIBAR Enable (DMIBAREN):** 0: DMIBAR is disabled and does not claim any memory. 1: DMIBAR memory mapped accesses are claimed and decoded appropriately.
28	R/W/L 0 b	**MCHBAR Enable (MCHBAREN):** 0: MCHBAR is disabled and does not claim any memory. 1: MCHBAR memory mapped accesses are claimed and decoded appropriately.
27	R/W/L 0 b	**EPBAR Enable (EPBAREN):** 0: EPBAR is disabled and does not claim any memory. 1: EPBAR memory mapped accesses are claimed and decoded appropriately.
26:5		**Reserved.**
4	R/W/L 1 b	**82915GM / 82915GME / 82910GML / 82910GMLE / 82915GMS :** **Internal Graphics Engine Function 1 (D2F1EN):** 0: Bus 0 Device 2 Function 1 is disabled and hidden 1: Bus 0 Device 2 Function 1 is enabled and visible **NOTE:** *If Device 2 Function 0 is disabled and hidden, then Device 2 Function 1 is also disabled and hidden independent of the state of this bit.* **82915PM:** Reserved.
3	R/W/L 1 b	**82915GM / 82915GME / 82910GML / 82910GMLE / 82915GMS :** **Internal Graphics Engine Function 0 (D2F0EN):** 0: Bus 0 Device 2 Function 0 is disabled and hidden 1: Bus 0 Device 2 Function 0 is enabled and visible **NOTE:** If this GMCH does not have internal graphics capability (CAPID0[38] = 1) then Device 2 Function 0 is disabled and hidden independent of the state of this bit. **82915PM:** Reserved.
2		**Reserved**
1	R/W/L 1 b	**82915GM / 82915GME / 82915PM:** **PCI Express Graphics Attach (D1EN):** 0: Bus 0 Device 1 Function 0 is disabled and hidden 1: Bus 0 Device 1 Function 0 is enabled and visible The SDVO Presence HW strap determines default value. Device 1 is Disabled on Reset when the SDVO Presence strap is sampled high, and is enabled otherwise. **82915GMS / 82910GML / 82910GMLE:** Reserved.
0	RO 1 b	**Host Bridge:** Bus 0 Device 0 Function 0 may not be disabled and is therefore hardwired to 1.

4.1.18 PAM0—Programmable Attribute Map 0

PCI Device: 0
Address Offset: 90h
Default Value: 00h
Access: RO, R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS area from 0F0000h-0FFFFFh

The GMCH allows programmable memory attributes on 13 Legacy memory segments of various sizes in the 640 kB to 1 MB address range. Seven Programmable Attribute Map (PAM) Registers are used to support these features. Cacheability of these areas is controlled via the MTRR registers in the processor. Two bits are used to specify memory attributes for each memory segment. These bits apply to both host accesses and PCI initiator accesses to the PAM areas. These attributes are:

RE - Read Enable. When RE = 1, the CPU read accesses to the corresponding memory segment are claimed by the GMCH and directed to main memory. Conversely, when RE = 0, the host read accesses are directed to PCI_A.

WE - Write Enable. When WE = 1, the host write accesses to the corresponding memory segment are claimed by the GMCH and directed to main memory. Conversely, when WE = 0, the host write accesses are directed to PCI_A.

The RE and WE attributes permit a memory segment to be Read Only, Write Only, Read/Write, or disabled. For example, if a memory segment has RE = 1 and WE = 0, the segment is Read Only.

Each PAM Register controls two regions, typically 16 kB in size.

Bit	Access & Default	Description
7:6		**Reserved.**
5:4	R/W 00 b	**0F0000-0FFFFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0F0000 to 0FFFFF. 00 = DRAM Disabled: All accesses are directed to DMI. 01 = Read Only: All reads are sent to DRAM. All writes are forwarded to DMI. 10 = Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11 = Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:0		**Reserved**

Warning: The GMCH may hang if a PCI Express Graphics Attach or DMI originated access to Read Disabled or Write Disabled PAM segments occur (due to a possible IWB to non-DRAM). For these reasons the following critical restriction is placed on the programming of the PAM regions:

At the time that a DMI or PCI Express Graphics Attach accesses to the PAM region may occur, the targeted PAM segment must be programmed to be both readable and writeable.

4.1.19 PAM1—Programmable Attribute Map 1

PCI Device: 0
Address Offset: 91h
Default Value: 00h
Access: RO, R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0C0000h-0C7FFFh.

Bit	Access & Default	Description
7:6		**Reserved.**
5:4	R/W 00 b	**0C4000-0C7FFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C4000 to 0C7FFF. 00:DRAM Disabled: Accesses are directed to DMI. 01:Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10:Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11:Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		**Reserved.**
1:0	R/W 00 b	**0C0000-0C3FFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C0000 to 0C3FFF. 00:DRAM Disabled: Accesses are directed to DMI. 01:Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10:Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11:Normal DRAM Operation: All reads and writes are serviced by DRAM.

4.1.20 PAM2—Programmable Attribute Map 2

PCI Device: 0
Address Offset: 92h
Default Value: 00h
Access: RO, R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0C8000h-0CFFFFh.

Bit	Access & Default	Description
7:6		**Reserved.**
5:4	R/W 00 b	**0CC000-0CCFFF Attribute (HIENABLE):** 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		**Reserved**
1:0	R/W 00 b	**0C8000-0CBFFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0C8000 to 0CBFFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.

4.1.21 PAM3—Programmable Attribute Map 3

PCI Device: 0
Address Offset: 93h
Default Value: 00h
Access: RO, R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0D0000h-0D7FFFh.

Bit	Access & Default	Description
7:6		**Reserved**
5:4	R/W 00 b	**0D4000-0D7FFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D4000 to 0D7FFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		**Reserved**
1:0	R/W 00 b	**0D0000-0D3FFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D0000 to 0D3FFF. **00**: DRAM Disabled: Accesses are directed to DMI. **01**: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. **10**: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. **11**: Normal DRAM Operation: All reads and writes are serviced by DRAM.

4.1.22 PAM4—Programmable Attribute Map 4

PCI Device: 0
Address Offset: 94h
Default Value: 00h
Access: RO, R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0D8000h-0DFFFFh.

Bit	Access & Default	Description
7:6		**Reserved**
5:4	R/W 00 b	**0DC000-0DFFFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0DC000 to 0DFFFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		**Reserved**
1:0	R/W 00 b	**0D8000-0DBFFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0D8000 to 0DBFFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.

4.1.23 PAM5—Programmable Attribute Map 5

PCI Device: 0
Address Offset: 95h
Default Value: 00h
Access: RO, R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0E0000h-0E7FFFh.

Bit	Access & Default	Description
7:6		**Reserved**
5:4	R/W 00 b	**0E4000-0E7FFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E4000 to 0E7FFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		**Reserved**
1:0	R/W 00 b	**0E0000-0E3FFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E0000 to 0E3FFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.

4.1.24 PAM6—Programmable Attribute Map 6

PCI Device: 0
Address Offset: 96h
Default Value: 00h
Access: RO, R/W
Size: 8 bits

This register controls the read, write, and shadowing attributes of the BIOS areas from 0E8000h-0EFFFFh.

Bit	Access & Default	Description
7:6		**Reserved**
5:4	R/W 00 b	**0EC000-0EFFFF Attribute (HIENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E4000 to 0E7FFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.
3:2		**Reserved**
1:0	R/W 00 b	**0E8000-0EBFFF Attribute (LOENABLE):** This field controls the steering of read and write cycles that address the BIOS area from 0E0000 to 0E3FFF. 00: DRAM Disabled: Accesses are directed to DMI. 01: Read Only: All reads are serviced by DRAM. All writes are forwarded to DMI. 10: Write Only: All writes are sent to DRAM. Reads are serviced by DMI. 11: Normal DRAM Operation: All reads and writes are serviced by DRAM.

4.1.25 LAC—Legacy Access Control

PCI Device: 0
Address Offset: 97h
Default Value: 00h
Access: RO, R/W
Size: 8 bits

This 8-bit register controls a fixed DRAM hole from 15-16 MB.

Bit	Access & Default	Description
7	R/W 0 b	**Hole Enable (HEN):** This field enables a memory hole in DRAM space. The DRAM that lies "behind" this space is not remapped. 0: No memory hole. 1: Memory hole from 15 MB to 16 MB.
6:1		Reserved.
0	R/W 0 b	**MDA Present (MDAP):** This bit works with the VGA Enable bits in the BCTRL register of device 1 to control the routing of CPU initiated transactions targeting MDA compatible I/O and memory address ranges. This bit should not be set if device 1's VGA Enable bit is not set. If device 1's VGA enable bit is not set, then accesses to IO address range x3BCh-x3BFh are forwarded to DMI. If the VGA enable bit is set and MDA is not present, then accesses to IO address range x3BCh-x3BFh are forwarded to PCI Express Graphics if the address is within the corresponding IOBASE and IOLIMIT, otherwise they are forwarded to DMI. MDA resources are defined as the following: Memory: 0B0000h - 0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, (including ISA address aliases, A[15:10] are not used in decode) Any I/O reference that includes the I/O locations listed above, or their aliases, will be forwarded to DMI even if the reference includes I/O locations not listed above. The following table shows the behavior for all combinations of MDA and VGA:

VGAEN	MDAP	Description
0	0	All References to MDA and VGA space are routed to HI
0	1	Illegal combination
1	0	All VGA and MDA references are routed to PCI Express Graphics Attach.
1	1	All VGA references are routed to PCI Express Graphics Attach. MDA references are routed to HI

4.1.26 TOLUD—Top of Low Used DRAM Register

PCI Device: 0
Address Offset: 9Ch
Default Value: 08h
Access: RO, R/W
Size: 8 bits

This 8-bit register defines the Top of Usable DRAM (TOLUD). Graphics Stolen Memory and TSEG are within dram space defined under TOLUD. From the top of low used DRAM, GMCH claims 1 to 64 MB of dram for internal graphics if enabled and 1, 2 or 8 MB of DRAM for TSEG if enabled.

Bit	Access & Default	Description
7:3	R/W 01 h	**Top of Low Usable Dram (TOUD)-R/W** This register contains bits 31 to 27 of an address one byte above the maximum DRAM memory that is usable by the operating system. Address bits 31 to 27 programmed to a "01h" implies a minimum memory size of 128 MB. Configuration software must set this value to the smaller of the following two choices: - Maximum amount of memory in the system plus one byte - Minimum address allocated for PCI memory Address bits 26:0 are assumed to be 000_0000h for the purposes of address comparison. The Host interface positively decodes an address towards dram if the incoming address is less than that value programmed in this register. This register must **not** be set to 0000 0 b. Note that the Top of Usable Dram is the lowest address above both Graphics Stolen memory and TSEG. The host interface determines the base of Graphics Stolen memory by subtracting the graphics stolen memory size from TOLUD and further decrements by TSEG size to determine base of TSEG.
2:0		Reserved.

Programming Example (for 82915GM, 82915GMS, 82915GME, 82910GML, 82910GMLE GMCH only):

- C1DRB7 is set to 4 GB
- TSEG is enabled and TSEG size is set to 1 MB
- Internal Graphics is enabled and Graphics Mode Select is set to 32 MB
- BIOS knows the OS requires 1G of PCI space

The BIOS also knows the range from FEC0_0000h to FFFF_FFFFh is not usable by the system. This 20-MB range at the very top of addressable memory space is lost to APIC.

According to the above equation, TOLUD is originally calculated to: 4 GB = 1_0000_0000h

The system memory requirements are:
4 GB (max addressable space) – 1 GB (PCI space) - 20 MB (lost memory) = 3 GB - 128 MB (minimum granularity) = B800_0000h

Since B800_0000h (PCI and other system requirements) is less than 1_0000_0000h; TOLUD should be programmed to B8h.

4.1.27 SMRAM—System Management RAM Control

PCI Device: 0
Address Offset: 9Dh
Default Value: 02h
Access: RO, R/W/L
Size: 8 bits

The SMRAMC register controls how accesses to Compatible and Extended SMRAM spaces are treated. The Open, Close, and Lock bits function only when G_SMRAME bit is set to a 1. Also, the OPEN bit must be reset before the LOCK bit is set.

Bit	Access & Default	Description
7		Reserved.
6	R/W/L 0 b	**SMM Space Open (D_OPEN):** (When D_OPEN=1 and D_LCK=0, the SMM space DRAM is made visible even when SMM decode is not active. This is intended to help BIOS initialize SMM space. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time.
5	R/W/L 0 b	**SMM Space Closed (D_CLS):** When D_CLS = 1 SMM space DRAM is not accessible to data references, even if SMM decode is active. Code references may still access SMM space DRAM. This will allow SMM software to reference through SMM space to update the display even when SMM is mapped over the VGA range. Software should ensure that D_OPEN=1 and D_CLS=1 are not set at the same time. Note that the D_CLS bit only applies to Compatible SMM space.
4	R/W/L 0 b	**SMM Space Locked (D_LCK):** When D_LCK is set to 1 then D_OPEN is reset to 0 and D_LCK, D_OPEN, C_BASE_SEG, H_SMRAM_EN, TSEG_SZ and TSEG_EN become read only. D_LCK can be set to 1 via a normal configuration space write but can only be cleared by a Full Reset. The combination of D_LCK and D_OPEN provide convenience with security. The BIOS can use the D_OPEN function to initialize SMM space and then use D_LCK to "lock down" SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the D_OPEN function.
3	R/W 0 b	**Global SMRAM Enable (G_SMRARE):** If set to a 1, then Compatible SMRAM functions are enabled, providing 128 KB of DRAM accessible at the A0000h address while in SMM (ADSB with SMM decode). To enable Extended SMRAM function this bit has be set to 1. Refer to the section on SMM for more details. Once D_LCK is set, this bit becomes read only.
2:0	RO 010 b	**Compatible SMM Space Base Segment (C_BASE_SEG)**: This field indicates the location of SMM space. SMM DRAM is not remapped. It is simply made visible if the conditions are right to access SMM space, otherwise the access is forwarded to DMI. Since the GMCH supports only the SMM space between A0000 and BFFFF, this field is hardwired to 010.

4.1.28 ESMRAMC—Extended System Management RAM Control

PCI Device: 0
Address Offset: 9Eh
Default Value: 38h
Access: RO, R/W, R/WC, R/W/L
Size: 8 bits

The Extended SMRAM register controls the configuration of Extended SMRAM space. The Extended SMRAM (E_SMRAM) memory provides a write-back cacheable SMRAM memory space that is above 1 MB.

Bit	Access & Default	Description
7	R/W 0 b	**Enable High SMRAM (H_SMRAME):** Controls the SMM memory space location (i.e. above 1 MB or below 1 MB) when G_SMRAME is 1 and H_SMRAME this bit is set to 1, the high SMRAM memory space is enabled. SMRAM accesses within the range 0FEDA0000h to 0FEDBFFFFh are remapped to DRAM addresses within the range 000A0000h to 000BFFFFh. Once D_LCK has been set, this bit becomes read only.
6	R/W/C 0 b	**Invalid SMRAM Access (E_SMERR):** This bit is set when CPU has accessed the defined memory ranges in Extended SMRAM (High Memory and T-segment) while not in SMM space and with the D-OPEN bit = 0. It is software's responsibility to clear this bit. The software must write a 1 to this bit to clear it.
5	RO 1 b	**SMRAM Cacheable (SM_CACHE):** This bit is forced to 1 by the GMCH .
4	RO 1 b	**L1 Cache Enable for SMRAM (SM_L1):** This bit is forced to 1 by the GMCH.
3	RO 1 b	**L2 Cache Enable for SMRAM (SM_L2):** This bit is forced to 1 by the GMCH.
2:1	R/W 00 b	**TSEG Size (TSEG_SZ):** Selects the size of the TSEG memory block if enabled. Memory from the top of DRAM space is partitioned away so that it may only be accessed by the processor interface and only then when the SMM bit is set in the request packet. Non-SMM accesses to this memory region are sent to DMI when the TSEG memory block is enabled. **00** - 1MB TSEG. (TOLUD – Graphics Stolen Memory Size – 1M) to (TOLUD – Graphics Stolen Memory Size). **01** - 2MB TSEG (TOLUD – Graphics Stolen Memory Size – 2M) to (TOLUD – Graphics Stolen Memory Size). **10** - 8 MB TSEG (TOLUD – Graphics Stolen Memory Size – 8M) to (TOLUD – Graphics Stolen Memory Size). **11** - Reserved. Once D_LCK has been set, these bits becomes read only.
0	R/W/L 0 b	**TSEG Enable (T_EN):** Enabling of SMRAM memory for Extended SMRAM space only. When G_SMRAME =1 and TSEG_EN = 1, the TSEG is enabled to appear in the appropriate physical address space. Note that once D_LCK is set, this bit becomes read only.

4.1.29 ERRSTS—Error Status

PCI Device: 0
Address Offset: C8h
Default Value: 0000h
Access: RO, R/WC
Size: 16 bits

This register is used to report various error conditions via the SERR messaging mechanism. An SERR message is generated on a zero to one transition of any of these flags (if enabled by the ERRCMD and PCICMD registers). These bits are set regardless of whether or not the SERR is enabled and generated. After the error processing is complete, the error logging mechanism can be unlocked by clearing the appropriate status bit by software writing a 1 to it.

Bit	Access & Default	Description
15:13		**Reserved**
12	R/WC 0 b	**GMCH Software Generated Event for SMI:** This indicates the source of the SMI was a Device 2 Software Event.
11	R/WC 0 b	**GMCH Thermal Sensor Event for SMI/SCI/SERR:** Indicates that a GMCH Thermal Sensor trip has occurred and an SMI, SCI, or SERR has been generated. The status bit is set only if a message is sent based on Thermal event enables in Error command, SMI command and Sci command registers. A trip point can generate one of SMI, SCI, or SERR interrupts (two or more per event is illegal). Multiple trip points can generate the same interrupt, if software chooses this mode, subsequent trips may be lost. If this bit is already set, then an interrupt message will not be sent on a new thermal sensor event.
10		**Reserved**
9	R/WC 0 b	**LOCK to non-DRAM Memory Flag (LCKF):** When this bit is set to 1, the GMCH has detected a lock operation to memory space that did not map into DRAM.
8	R/WC 0 b	**Received Refresh Timeout Flag(RRTOF):** This bit is set when 1024 memory core refreshes are enqueued.
7	R/WC 0 b	**DRAM Throttle Flag (DTF):** 1: Indicates that a DRAM Throttling condition occurred. 0: Software has cleared this flag since the most recent throttling event
6:0		**Reserved.**

4.1.30 ERRCMD—Error Command

PCI Device: 0
Address Offset: CAh
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register controls the GMCH responses to various system errors. Since the GMCH does not have an SERRB signal, SERR messages are passed from the GMCH to the ICH over DMI. When a bit in this register is set, a SERR message will be generated on DMI whenever the corresponding flag is set in the ERRSTS register. The actual generation of the SERR message is globally enabled for Device #0 via the PCI Command register.

Bit	Access & Default	Description
15:12		**Reserved**
11	R/W 0 b	**SERR on GMCH Thermal Sensor Event (TSESERR):** 1: The GMCH generates a SERR when bit 11 of the ERRSTS is set. The SERR must not be enabled at the same time as the SMI for the same thermal sensor event. 0: Reporting of this condition via SERR messaging is disabled.
10	R/W 0 b	**Reserved**
9	R/W 0 b	**SERR on LOCK to non-DRAM Memory (LCKERR):** 1: The GMCH will generate a SERR special cycle whenever a CPU lock cycle is detected that does not hit DRAM. 0: Reporting of this condition via SERR messaging is disabled.
8	R/W 0 b	**SERR on DRAM Refresh Timeout (DRTOERR):** 1: The GMCH generates an SERR special cycle when a DRAM Refresh timeout occurs. 0: Reporting of this condition via SERR messaging is disabled.
7	R/W 0 b	**SERR on DRAM Throttle Condition (DTCERR):** 1: The GMCH generates an SERR DMI special cycle when a DRAM Read or Write Throttle condition occurs. 0: Reporting of this condition via SERR messaging is disabled.
6:0		**Reserved.**

4.1.31 SKPD—Scratchpad Data (D0:F0)

PCI Device: 0
Address Offset: DCh
Default Value: 00000000h
Access: R/W
Size: 32 bits

This register holds 32 writable bits with no functionality behind them. It is for the convenience of BIOS and graphics drivers.

Bit	Access & Default	Description
31:0	R/W 00000000 h	**Scratchpad Data:** 1 DWORD of data storage.

4.1.32 CAPID0—Capability Identifier

PCI Device: 0
Address Offset: E0h
Default Value: xxxxxxxxxxxx90009h
Access: RO
Size: 72 bits

Bit	Access & Default	Description
71:24	RO	**Intel Reserved**
23:16	RO 09 h	**CAPID Length:** This field has the value 09h to indicate the structure length (9 bytes).
15:8	RO 00 h	**Next Capability Pointer:** This field is hardwired to 00h indicating the end of the capabilities linked list.
7:0	RO 09 h	**CAP_ID:** This field has the value 1001b to identify the CAP_ID assigned by the PCI SIG for vendor dependent capability pointers.

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5 Device #0 Memory Mapped I/O Register

Note: All accesses to the Memory Mapped registers must be made as a single DWORD (4 bytes) or less. Access must be aligned on a natural boundary.

5.1 MCHBAR Registers Device #0

A variety of timing & control registers have been moved to MMR space of Device 0 due to space constraints.

To simplify the read/write logic to the SRAM, BIOS is required to write and read 32-b aligned Double Words. The SRAM includes a separate Write Enable for every Double Word.

The BIOS read/write cycles are performed in a memory mapped IO range that is setup for this purpose in the PCI configuration space, via std. PCI range scheme.

5.2 Device #0 MCHBAR Chipset Control Register Space

Address Offset (h)	Register Symbol	Register Name	Default Value	Access
000-039h		***Reserved***		
040h	HIC	Host Interface Configuration		
041-0FFh		***Reserved***		
100h	C0DRB0	Ch0 DRAM Rank Boundary Address 0	00h	R/W
101h	C0DRB1	Ch0 DRAM Rank Boundary Address 1	00h	R/W
102h	C0DRB2	Ch0 DRAM Rank Boundary Address 2	00h	R/W
103h	C0DRB3	Ch0 DRAM Rank Boundary Address 3	00h	R/W
104-107h		***Reserved***		
108h	C0DRA0	Ch0 DRAM Rank 0,1 Attribute	00h	RO, R/W
109h	C0DRA2	Ch0 DRAM Rank 2,3 Attribute	00h	RO, R/W
10A-10Bh		***Reserved***		
10Ch	C0DCLKDIS	Ch0 DRAM Clock Disable	00h	RO, R/W
10Dh		***Reserved***		
10E-10Fh	C0BNKARC	Ch0 Bank Architecture	0000h	RO, R/W
110-113h	C0DRT0	Ch0 DRAM Timing Register 0	A96000E8h	RO, R/W
114-117h	C0DRT1	Ch0 DRAM Timing Register 1	00006111h	RO, R/W
118-11Bh	C0DRT2	Ch0 DRAM Timing Register2	000003FFh	RO, R/W
11C-11Fh		***Reserved***		
120-123h	C0DRC0	Ch0 DRAM Controller Mode Register 0	00000000h	RO, R/W
124-127h	C0DRC1	Ch0 DRAM Controller Mode Register 1	00000000h	RO, R/W
138-13Bh	C0DRC2	Ch0 DRAM Controller Mode Register 2	00000000h	RO, R/W

Address Offset (h)	Register Symbol	Register Name	Default Value	Access
13C-157h		***Reserved***		
158-15Bh	C0DTC	Ch0 DRAM Throttling Control	00000000h	RO, R/L, R/W/L
15C-17Fh		***Reserved***		
180h	C1DRB0	Channel 1 DRAM Rank Boundary Address 0	00h	R/W
181h	C1DRB1	Channel 1 DRAM Rank Boundary Address 1	00h	R/W
182h	C1DRB2	Channel 1 DRAM Rank Boundary Address 2	00h	R/W
183h	C1DRB3	Channel 1 DRAM Rank Boundary Address 3	00h	R/W
184-187h		***Reserved***		
188h	C1DRA0	Channel 1 Dram Rank 0,1 Attribute	00h	RO, R/W
189h	C1DRA2	Channel 1 Dram Rank 2,3 Attribute	00h	RO, R/W
18A-18Bh		***Reserved***		
18Ch	C1DCLKDIS	Channel 1 DRAM Clock Disable	00h	RO, R/W
18Dh		***Reserved***		
18E-18Fh	C1BNKARC	Channel 1 Bank Architecture	0000h	RO, R/W
190-193h	C1DRT0	Channel 1 DRAM Timing Register 0	A96000E8h	RO, R/W
194-197h	C1DRT1	Channel 1 DRAM Timing Register 1	00006111h	RO, R/W
198-19Bh	C1DRT2	Channel 1 DRAM Timing Register 2	000003FFh	RO, R/W
19C-19Fh		***Reserved***		
1A0-1A3h	C1DRC0	Channel 1 DRAM Controller Mode 0	40002801h	RO, R/W
1A4-1A5h	C1DRC1	Channel 1 DRAM Controller Mode 1	00000000h	RO, R/W
1A6-1A7h		***Reserved***		
1A8-1AFh	C1DRC2	Channel 1 DRAM Controller Mode 2	00000000h	RO, R/W
1B0-1D7h		***Reserved***		
1D8-1DBh	C1DTC	Channel 1 DRAM Throttling Control	00000000h	RO, R/L, R/W/L
1DC-1FFh		***Reserved***		
200-203h	DCC	DRAM Channel Control	00000000h	RO, R/W
204-27Fh		***Reserved***		

5.2.1 HIC Host Interface Configuration Register

PCI Device: MCHBAR
Address Offset: 040h
Size: 32 bits

Bit	Access & Default	Description
31:9		Reserved
8	RO 0b	**PCI Express Graphics / SDVO strap bit** – Specifies the use of the PCI Express bus for external graphics muxed with DVO. 0: SDVO disabled. PCI Express is available. 1: SDVO enabled. PCI Express is disabled.
7:2		Reserved
1	RW 0b	**Dispatch Disable:** 0: Enables dispatch of qualified CPU-to-DRAM read requests in FSB. 1: Dispatch occurs no sooner than T3. **Note:** BIOS must set this bit to a 1 before starting DRAM initialization. BIOS can set this bit to 0 after DRAM initialization is complete.
0		**Reserved**

5.2.2 HIT1—Host Interface Test_1

PCI Device: MCHBAR
Address Offset: 044h
Size: 32 bits

Bit	Access & Default	Description
31:6		**Reserved**
5	R/W 0 b	**Front Side Bus Power Management Enable.** 0 = FSB Power Management Disabled (Default). 1 = FSB Power Management Enabled.
4	R/W 0 b	**C2 FSB Power Management Enable** 0 = C2 FSB Power Management Disabled. 1 = C2 FSB Power Management Enabled.
3:0		**Reserved**

5.2.3 C0DRB0—Channel 0 DRAM Rank Boundary 0

PCI Device: MCHBAR
Address Offset: 100h
Default Value: 00h
Access: R/W
Size: 8 bits

The **DRAM Rank Boundary Register** defines the upper boundary address of each DRAM rank with a granularity of 128 MB (256 Mbit, X16 devices). Each rank has its own single-byte **DRB** register. These registers are used to determine which chip select will be active for a given address.

Channel and rank map:

ch0 rank0: 100h
ch0 rank1: 101h
ch0 rank2: 102h
ch0 rank3: 103h
Reserved: 104h to 107h

In all modes, if a SO-DIMM is single-sided it appears as a populated rank and an empty rank. A DRB must be programmed appropriately for each.

Each Rank is represented by a byte. Each byte has the following format.

Bit	Access & Default	Description
7:0	R/W 00 h	**Channel 0 DRAM Rank Boundary Address:** This 8 bit value defines the upper and lower addresses for each DRAM rank. Bits 6:2 are compared against Address 31:27 to determine the upper address limit of a particular rank. Bits 1:0 must be 0s. Bit 7 may be programmed to a 1 in the highest DRB (DRB3) if 4 GB of memory is present.

5.2.4 C0DRB1—Channel 0 DRAM Rank Boundary 1

PCI Device: MCHBAR
Address Offset: 101h
Default Value: 00h
Access: R/W
Size: 8 bits

The operation of this register is detailed in the description for register C0DRB0.

5.2.5 C0DRB2—Channel 0 DRAM Rank Boundary 2

PCI Device: MCHBAR
Address Offset: 102h
Default Value: 00h
Access: R/W
Size: 8 bits

The operation of this register is detailed in the description for register C0DRB0.

5.2.6 C0DRB3—Channel 0 DRAM Rank Boundary 3

PCI Device: MCHBAR
Address Offset: 103h
Default Value: 00h
Access: R/W
Size: 8 bits

The operation of this register is detailed in the description for register C0DRB0.

5.2.7 C0DRA0—Channel 0 DRAM Rank 0,1 Attribute

PCI Device: MCHBAR
Address Offset: 108h
Default Value: 00h
Access: RO, R/W
Size: 8 bits

The **DRAM Rank Attribute Registers** define the page sizes to be used when accessing different ranks. These registers should be left with their default value (all zeros) for any rank that is unpopulated, as determined by the corresponding CxDRB registers. Each byte of information in the **CxDRA** registers describes the page size of a pair of ranks.

Channel and rank map:

Ch0 Rank0, 1: 108h

Ch0 Rank2, 3: 109h

Reserved. 10Ah, 10Bh:

Bit	Access & Default	Description
7		Reserved
6:4	R/W 000 b	**Channel 0 DRAM odd Rank Attribute:** This 3-bit field defines the page size of the corresponding rank. 000: Unpopulated. 001: Reserved 010: 4 kB 011: 8 kB 100: 16 kB Others: Reserved
3		Reserved
2:0	R/W 000 b	**Channel 0 DRAM even Rank Attribute:** This 3-bit field defines the page size of the corresponding rank. 000: Unpopulated. 001: Reserved 010: 4 kB 011: 8 kB 100: 16 kB Others: Reserved

5.2.8 C0DRA2—Channel 0 DRAM Rank 2,3 Attribute

PCI Device: MCHBAR
Address Offset: 109h
Default Value: 00h
Access: RO, R/W
Size: 8 bits

The operation of this register is detailed in the description for register C0DRA0.

5.2.9 C0DCLKDIS—Channel 0 DRAM Clock Disable

MMIO Range: MCHBAR
Address Offset: 10Ch
Default Value: 00h
Access: RO, R/W
Size: 8 bits

This register can be used to disable the System Memory Clock signals to each SO-DIMM slot, which can significantly reduce EMI and Power concerns for clocks that go to unpopulated SO-DIMM s. Clocks should be enabled based on whether a slot is populated.

Bit	Access & Default	Description
7:3	RO 00 b	**Reserved**
2	R/W 0 b	**DIMM clock gate enable pair 2 - (Reserved)** 0: Tri-state the corresponding clock pair. 1: Reserved
1	R/W 0 b	**DIMM clock gate enable pair 1** 0: Tri-state the corresponding clock pair. 1: Enable the corresponding clock pair.
0	R/W 0 b	**DIMM clock gate enable pair 0** 0: Tri-state the corresponding clock pair. 1: Enable the corresponding clock pair.

Note: Since there are multiple clock signals assigned to each rank of a SO-DIMM , it is important to clarify exactly which rank width field affects which clock signal:

Channel	Rank	Clocks Affected
0	0 or 1	SM_CK[2:0] / SM_CK#[1:0]
1	2 or 3	SM_CK[4:3] / SM_CK#[4:3]

5.2.10 C0BNKARC—Channel 0 DRAM Bank Architecture

PCI Device: MCHBAR
Function: 0
Address Offset: 10Eh
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register is used to program the bank architecture for each Rank

Bit	Access & Default	Description
15:8	RO 00 h	**Reserved**
7:6	R/W 00 b	**Rank 3 Bank Architecture** 00: 4 Banks. 01: 8 Banks. 1X: Reserved
5:4	R/W 00 b	**Rank 2 Bank Architecture** 00: 4 Banks. 01: 8 Banks. 1X: Reserved
3:2	R/W 00 b	**Rank 1 Bank Architecture** 00: 4 Banks. 01: 8 Banks. 1X: Reserved
1:0	R/W 00 b	**Rank 0 Bank Architecture** 00: 4 Banks. 01: 8 Banks. 1X: Reserved

5.2.11 C0DRT0—Channel 0 DRAM Timing Register 0

PCI Device: MCHBAR
Address Offset: 110h
Default Value: A96000E8
Access: RO, R/W
Size: 32 bits

This 32-bit register defines the timing parameters for all devices in this channel. The BIOS programs this register with the "least common denominator" values for each channel after reading configuration registers of each device in each channel.

Bit	Access & Default	Description
31:28	R/W A h	**Back To Back Write To Precharge Command Spacing (Same bank):** This field determines the number of clocks between write command and a subsequent pre-charge command to the same bank. The minimum number of clocks is calculated based on this formula: **DDR 2 :- CL – 1 + BL/2 + tWR** **DDR :- 1 + BL/2 + tWR** 0000 – 0100: Reserved 1110 – 1111 Reserved **NOTE:** Write Recovery time (tWR). Write recovery time is a standard DDR/DDR 2 timing parameter that determines minimum time between a write command and a subsequent precharge command to the same bank. This parameter is programmable on DDR 2 SO-DIMM s and the value used above must match the largest delay programmed in any SO-DIMM in the system. Minimum recommended values are documented below. tWR (on CK) 3 Clocks – DDR 333 or DDR 2 400 4 Clocks – DDR 2 533
27:24	R/W 9 h	**Back To Back Write To Read Command Spacing (Same rank):** This field determines the number of clocks between write command and a subsequent read command to the same rank. The minimum number of clocks is calculated based on this formula **DDR 2 :- CL – 1 + BL/2 + tWTR** **DDR :- 1 + BL/2 + tWTR** 0000 – 0011 Reserved 1100 – 1111 Reserved **NOTE:** Write to Read Command delay (tWTR). The tWTR is a standard DDR timing parameter with a value of 1 clock for DDR CL=2 or CL=2.5 and a value of 2 clocks for DDR CL=1.5 or any CL for DDR 2 400/533. The tWTR is used to time a RD command after a WR command to the same row. 1 Clocks – CL = 2 or CL = 2.5 for DDR 333 2 Clocks – CL = 1.5 or DDR2 400, DDR2 533

Bit	Access & Default	Description
23:22	R/W 01 b	**Back To Back Write-Read Command Spacing (Different Rank):** This field determines the number of turn-around clocks on the data bus needs to be inserted between write command and a subsequent read command. The minimum spacing of commands is calculated based on the formula **DDR 2 = BL/2 + TA –1** *(Derived from: DDR 2 = BL/2 + **TA** (wr-rd) + WL – CL* *DDR 2 = BL/2 + **TA** + CL –1 – CL)* **DDR = Ceiling(DQSS + BL/2 + TA (wr-rd) - CL);** DQSS: is the time from the write command to the associated data and is always 1 CK in DDR BL: is the burst length 8 TA: is the required write to read DQ turn-around on the bus can be set to 1, 2, or 3 CK using this register. CL: is CAS latency **Encoding BL8 CMD Spacing** 00: 6 01: 5 10: 4 11: 3 (DDR only)
21:20	R/W 10 b	**Back To Back Read-Write Command Spacing:** This field determines the # of turn-around clocks between the read command and a subsequent write command The minimum spacing of commands is calculated based on the formula **DDR 2 :- BL/2 + TA +1** *(DDR 2 :- CL + BL/2 + TA (wr-rd) – WL* *DDR 2 :- CL + BL/2 + TA – CL +1)* **DDR :- Ceiling (CL + BL/2 + TA – 1)** BL: is the burst length 8 TA: is the required read to write DQ turn-around on the bus can be set to 1, 2, 3, 4 CK for DDR 2 and can be set to 1, 2, 3 CK for DDR CL: is CAS latency **Encoding BL8 CMD Spacing** 00: 9 01: 8 10: 7 11: 6 The bigger turn-around are used in large configurations, where the difference in total channel delay between the fastest and slowest SO-DIMM is large.
19:18	R/W 00 b	**Back To Back Write Command Spacing:** This field controls the turnaround time on the DQ bus for WR-WR sequence to different ranks in one channel. The minimum spacing of commands is calculated based on the formula **DDR 2 and DDR = BL/2 + TA** **Encoding Turn-Around BL8 CMD Spacing** 00: 2 turnaround clocks on DQ 6 01: 1 turnaround clocks on DQ 5

Bit	Access & Default	Description
		10: 0 turnaround clocks on DQ 4 11: Reserved The bigger turn-around are used in large configurations, where the difference in total channel delay between the fastest and slowest SO-DIMM is large.
17	RO 0 b	**Reserved**
16	R/W 0 b	Back To Back Read Command Spacing: This field controls the turnaround time on the DQ bus for RD-RD sequence to different ranks in one channel. The minimum spacing of commands is calculated based on the formula DDR 2 and DDR = BL/2 + TA Encoding Turn-Around BL8 CMD Spacing 0: 2 turnaround clocks on DQ 6 1: 1 turnaround clocks on DQ 5 The bigger turn-around are used in large configurations, where the difference in total channel delay between the fastest and slowest SO-DIMM is large.
15:11	R/W 00 h	Read Delay (tRD). tRD is the number of memory clocks from CS# assert to HDRDY# assertion on the FSB. The following tRD values are supported: 00000 – 00010: Reserved. 00011: 3 mclks 00100: 4 mclks 00101: 5 mclks 00110: 6 mclks 00111: 7 mclks 01000: 8 mclks 01001: 9 mclks 01010: 10 mclks ... 11110: 30 mclks 11111: 31 mclks
10:9	RO 00 b	Reserved
8:4	R/W 01111 b	Write Auto pre-charge to Activate (Same bank) This field determines the clock spacing between write command with Auto pre-charge and a subsequent Activate command to the same bank. The minimum spacing is calculated based on this formula: DDR 2 = CL -1 + BL/2 + tWR + tRP DDR = 1 + BL/2 + tWR + tRP 00000 - 00011: Reserved 00100 – 10011: Allowed 10100 – 11111: Reserved. Note: tWR is a Dram Parameter.
3:0	R/W	Read Auto pre-charge to Activate (Same bank)

Bit	Access & Default	Description
	8 h	This field determines the clock spacing between read command with Auto pre-charge and a subsequent Activate command to the same bank. The minimum spacing is calculated based on this formula: DDR 2 = tRTPC + tRP DDR = tRTPC + tRP Note tRTPC is defined in XXDRT1 bits 29:28.

5.2.12 C0DRT1—Channel 0 DRAM Timing Register 1

PCI Device: MCHBAR
Address Offset: 114h
Default Value: 00006111h
Access: RO, R/W
Size: 32 bits

<table>
<tr><th>Bit</th><th>Access & Default</th><th>Description</th></tr>
<tr><td>31:30</td><td></td><td>Reserved</td></tr>
<tr><td>29:28</td><td>R/W
00 b</td><td>Read to Pre-charge (tRTPC).
These bits control the number of clocks that are inserted between a read command to a row pre-charge command to the same rank.
Encoding tRP
00: BL/2
01 - 11: Reserved</td></tr>
<tr><td>27:24</td><td></td><td>Reserved</td></tr>
<tr><td>23:20</td><td>R/W
6 h</td><td>Activate to Precharge delay (tRAS).
This bit controls the number of DRAM clocks for tRAS. Minimum recommendations are beside their corresponding encodings.
Recommended values:
7h DDR 333
9h DDR 2 400
Ch DDR 2 533</td></tr>
<tr><td>19:18</td><td></td><td>Reserved</td></tr>
<tr><td>17</td><td>R/W
0 b</td><td>Activate to Activate delay:
Control Act to Act delay between the different banks of the same rank. Trr is specified in “ns”. 10ns for 2KB page size and 7.5 ns for 1KB page
0 = 2 Clock
1 = 3 Clock</td></tr>
<tr><td>16</td><td>R/W
0 b</td><td>Pre-All to Activate Delay (tRPALL).
This is applicable only to 8 bank architectures.
Must be set to 1 if any Rank is populated with 8 bank device technology.
0: tRPALL = tRP
1: tRPALL = tRP + 1</td></tr>
<tr><td>15:11</td><td>R/W
01100 b</td><td>Refresh Cycle Time (tRFC).
Refresh cycle time is measured from a Refresh command (REF) until the first Activate command (ACT) to the same rank, required to perform a read or write.
DDR 2 tRFC spec
<table>
<tr><th>tRFC</th><th>256Mb</th><th>512Mb</th><th>1Gb</th></tr>
<tr><td>DDR2 400 (5ns)</td><td>75 ns = 15 clks</td><td>105 ns = 21 clks</td><td>127.5 ns = 26 clks</td></tr>
<tr><td>DDR2 533 (3.75ns)</td><td>75 ns = 20 clks</td><td>105 ns = 28 clks</td><td>127.5 ns = 34clks</td></tr>
</table>
DDR 1 tRFC spec
<table>
<tr><th>tRFC</th><th>64Mb -512Mb</th><th>1Gb</th></tr>
<tr><td>DDR 333 (6ns)</td><td>75 ns = 13 clks</td><td>120 ns = 20 clks</td></tr>
</table>
00000b – 11111b Zero Clocks to Thirty-one Clocks respectively
Actual clocks period depends on DDR clock frequency.
Bios should round up. If the required clock count exceeds as allowed by this register, the bios should set this register to the max value and set corresponding bits in SDBUP.</td></tr>
<tr><td>10</td><td>RO</td><td>Reserved</td></tr>
</table>

Bit	Access & Default	Description
9:8	R/W 01 b	**CASB Latency (tCL).** This value is programmable on DDR 2 SO-DIMM's. The value programmed here must match the CAS Latency of every DDR 2 SO-DIMM in the system. Encoding DDR CL DDR 2 CL 00: 3 5 01: 2.5 4 10: Reserved 3 11: Reserved Reserved
7	RO	**Reserved**
6:4	R/W 001 b	**DRAM RASB to CASB Delay (tRCD).** This bit controls the number of clocks inserted between a row activate command and a read or write command to that row. Encoding tRCD 000: 2 DRAM Clocks 001: 3 DRAM Clocks 010: 4 DRAM Clocks 011: 5 DRAM Clocks 100 - 111: Reserved
3	RO	**Reserved**
2:0	R/W 001 b	**DRAM RASB Precharge (tRP).** This bit controls the number of clocks that are inserted between a row precharge command and an activate command to the same rank. Encoding tRP 000: 2 DRAM Clocks 001: 3 DRAM Clocks 010: 4 DRAM Clocks 011: 5 DRAM Clocks 100 - 111: Reserved

5.2.13 C0DRT2—Channel 0 DRAM Timing Register 2

PCI Device: MCHBAR
Address Offset: 118h
Default Value: 0000003FFh
Access: RO, R/W
Size: 32 bits

Bit	Access & Default	Description
31:30	R/W 00 b	**CKE Deassert Duration** 00 = 1 clk **(DDR)** 01 = Reserved 10 = 3 clk **(DDR2)** **11 = Reserved** **Must be set to 10 for DDR2**
29:18		**Reserved**
17:16	RW 00 b	**Reserved**
15:10	RO 00 h	**Reserved**
9:8	R/W 11 b	**Power Down Exit to CS# active time (tXPDN).** Power down exit time is tracked from the clock in which we sample CKE active, after exit from dynamic power down, until the clock which we drive a command (ACT/PRE/RD/WR). Exit time must be set to 1 clock for DDR and 2 for DDR2. Option to set exit time to 2 clocks for DDR is provided. 00 = Reserved. 01 = Reserved 10 = Power Down Exit time is set to 2 clocks 11 = Power Down Exit time is set to 1 clock
7:5	R/W 111 b	**DRAM Page Close Idle Timer:** This field determines the number of clocks a bank needs to remain unaccessed before dram controller considers it for pre-charge. 001 8 DRAM clocks 111 Infinite, Pages are left open. Other Reserved
4:0	R/W 11111 b	**DRAM Power down Idle Timer:** This field determines the number of clocks a rank remains unaccessed before the controller powers down that rank (CKE de-asserted). 01000b Recommended setting when using DDR2-533 MHz memory. 10000b Recommended setting when using DDR2-400 MHz memory. 11111b Infinite, CKE is not de-asserted based on the timer. Other Reserved

5.2.14 C0DRC0–-Channel 0 DRAM Controller Mode 0

PCI Device: MCHBAR
Address Offset: 120h
Default Value: 40002801h
Access: RO, R/W
Size: 32 bits

Bit	Access & Default	Description
31:30		**Reserved.**
29	R/W 0 b	**Initialization Complete (IC):** This bit is used for communication of software state between the memory controller and the BIOS. BIOS sets this bit to 1 after initialization of the DRAM memory array is complete.
28		**Reserved**
27:24	R/W 0 h	**Active SDRAM Ranks:** Implementations may use this field to limit the maximum number of SDRAM ranks that may be active at once. 0000: All ranks allowed to be in the active state 0001: One Rank 0010: Two Ranks 0011: Three Ranks Others: Reserved. If this field is set to a non-zero value, then bits CXDRT2(4:0) should be set to the minimum value as described by the formula, else the system hangs.
23:16		**Reserved**
15	R/W 0 b	**CMD copy enable (Single channel only)** In a single channel mode, the CMD pins (MA, BS, RAS, CAS, WE) on both channels are driven and are physical copies of each other. Setting this bit disables the CMD pins on channel B. Having the additional copy of CMD pins helps reduce loading on these pins, since in a two SO-DIMM system, each copy can be routed up to separate SO-DIMM. In a single DIMM system, the second copy can be disabled to eliminate unnecessary toggling of these pins. If this bit needs to be set, BIOS should do that before memory init sequence. This bit should not be set in a dual channel system
14:11		**Reserved**
10:8	R/W 000 b	**Refresh Mode Select (RMS):** This field determines whether refresh is enabled and, if so, at what rate refreshes will be executed. 000: Refresh disabled 001: Refresh enabled. Refresh interval 15.6 µs 010: Refresh enabled. Refresh interval 7.8 µs Other: Reserved
7	RO 0 b	**Reserved**
6:4	R/W 000 b	**Mode Select (SMS).** These bits select the special operational mode of the DRAM interface. The special modes are intended for initialization at power up. **000**: Post Reset state – When the GMCH exits reset (power-up or otherwise), the mode select field is cleared to 000. During any reset sequence, while power is applied and reset is active, the GMCH de-asserts all CKE signals. After internal reset is de-asserted, CKE signals

Bit	Access & Default	Description
		remain de-asserted until this field is written to a value different than “000”. On this event, all CKE signals are asserted. During suspend, GMCH internal signal triggers DRAM controller to flush pending commands and enter all ranks into Self-Refresh mode. As part of resume sequence, GMCH will be reset – which will clear this bit field to “000” and maintain CKE signals de-asserted. After internal reset is de-asserted, CKE signals remain de-asserted until this field is written to a value different than “000”. On this event, all CKE signals are asserted. During entry to other low power states (C3, S1), GMCH internal signal triggers DRAM controller to flush pending commands and enter all ranks into Self-Refresh mode. During exit to normal mode, GMCH signal triggers DRAM controller to exit Self-Refresh and resume normal operation without S/W involvement. **001:** NOP Command Enable – All CPU cycles to DRAM result in a NOP command on the DRAM interface. **010:** All Banks Pre-charge Enable – All CPU cycles to DRAM result in an “all banks precharge” command on the DRAM interface. **011:** Mode Register Set Enable – All CPU cycles to DRAM result in a “mode register” set command on the DRAM interface. Host address lines are mapped to DRAM address lines in order to specify the command sent. Host address lines [12:3] are mapped to MA[9:0], and HA[13] is mapped to MA[11]. **101**: Reserved **110:** **CBR Refresh Enable** – In this mode all CPU cycles to DRAM result in a CBR cycle on the DRAM interface **111:** Normal operation
3		**Reserved**
2	R/W 0 b	**Burst Length (BL):** The burst length is the number of QWORDS returned by a SO-DIMM per read command, when not interrupted. This bit is used to select the DRAM controller’s Burst Length operation mode. It must be set to match to the behavior of the SO-DIMM. 0: Burst Length of 4 1: Burst Length of 8
1:0	RO 01 b	**DRAM Type (DT)** Used to select between supported SDRAM types. 00: Reserved 01: Dual Data Rate (DDR) SDRAM 10: Dual Data Rate 2 (DDR 2) SDRAM 11: Reserved

5.2.15 C0DRC1––Channel 0 DRAM Controller Mode 1

PCI Device: MCHBAR
Address Offset: 124h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

Bit	Access & Default	Description
31:20		**Reserved**
19:16	R/W 0 h	**CKE Tri-state Enable Per Rank.** Bit 16 corresponds to rank 0 Bit 17 corresponds to rank 1 Bit 18 corresponds to rank 2 Bit 19 corresponds to rank3 0 = CKE is not tri-stated. 1 = CKE is tri-stated. This is set only if the Rank is physically not populated.
15:13		**Reserved**
12	R/W 0 b	**CS# Tri-state enable (CSBTRIEN):-** When set to a 1, the DRAM controller will tri-state CS# when the corresponding CKE is deasserted. 0: Address Tri-state Disabled 1: Address Tri-state Enabled
11	R/W 0 b	**Address Tri-state enable (ADRTRIEN):-** When set to a 1, the DRAM controller will tri-state the MA, CMD, and CSB (CSB if lines only when all CKEs are deasserted. CKEs deassert based on Idle timer or max rank count control. 0: Address Tri-state Disabled 1: Address Tri-state Enabled
10:9		**Reserved**
8	R/W 0 b	**DRAM Channel IO-Buffers Activate:** This bit is cleared to 0 during reset and remains inactive until it is set to 1 by BIOS. In addition, this bit can be cleared and set during debug procedures. **While 0**, the DRAM controller core logic forces the state of the IO-buffers in this channel to “reset” or “preset”, **While 1**, the DRAM controller core logic enables the DRAM IO-buffers in this channel to operate normally. **BIOS initialization Procedure:** This bit is cleared (0) during reset. It remains 0 after reset. BIOS is expected to use to following sequence: During and after platform reset, the DRAM controller core logic drives CKE to 0 and toggles clock output (drive strength and slew rate are set based on default values). After reset, BIOS detects DRAM configuration, through Serial Presence Detect. BIOS sets appropriate RCOMP values, then it performs initial RCOMP. BIOS enables the RCVEN, DQS and optionally CK DLL’s BIOS sets this bit (1), to enable normal operations. MA/BA/command are driven to default, CSB I driven inactive (data related outputs remain tri-stated, CKE remain 0 while clocks are toggled). Perform DRAM initialization, through SMS bit field (CKE is activated). Enable refresh. Enable periodic RCOMP. Both this bit must be 1 and SMS must be different than 000 for CKE to be activated. It is sufficient to clear this bit to 0 for CKE to go inactive.
7:0		**Reserved**

5.2.16 C0DRC2–-Channel 0 DRAM Controller Mode 2

PCI Device: MCHBAR
Address Offset: 128h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

Bit	Access & Default	Description
31:28		**Reserved**
27:24	R/W 0 h	**Dram ODT Tristate Enable Per Rank: DDR 2** Bit 24 corresponds to rank 0 Bit 25 corresponds to rank 1 Bit 26 corresponds to rank 2 Bit 27 corresponds to rank 3 0 = ODT is not tri-stated. 1 = ODT is tri-stated. This is set only if the Rank is physically not populated.
23:0		**Reserved**

5.2.17 C1DRB0—Channel 1 DRAM Rank Boundary Address 0

MMIO Range: MCHBAR
Address Offset: 180h
Default Value: 00h
Access: R/W
Size: 8 bits

The operation of this register is detailed in the description for register C0DRB0.

5.2.18 C1DRB1—Channel 1 DRAM Rank Boundary Address 1

MMIO Range: MCHBAR
Address Offset: 181h
Default Value: 00h
Access: R/W
Size: 8 bits

The operation of this register is detailed in the description for register C0DRB0.

5.2.19 C1DRB2—Channel 1 DRAM Rank Boundary Address 2

MMIO Range: MCHBAR
Address Offset: 182h
Default Value: 00h
Access: R/W
Size: 8 bits

The operation of this register is detailed in the description for register C0DRB0.

5.2.20 C1DRB3—Channel 1 DRAM Rank Boundary Address 3

MMIO Range: MCHBAR
Address Offset: 183h
Default Value: 00h
Access: R/W
Size: 8 bits

The operation of this register is detailed in the description for register C0DRB0.

5.2.21 C1DRA0—Channel 1 Dram Rank 0,1 Attribute

MMIO Range: MCHBAR
Address Offset: 188h
Default Value: 00h
Access: RO, R/W
Size: 8 bits

The operation of this register is detailed in the description for register C0DRA0.

5.2.22 C1DRA2—Channel 1 Dram Rank 2,3 Attribute

MMIO Range: MCHBAR
Address Offset: 189h
Default Value: 00h
Access: RO, R/W
Size: 8 bits

The operation of this register is detailed in the description for register C0DRA0.

5.2.23 C1DCLKDIS—Channel 1 DRAM Clock Disable

MMIO Range: MCHBAR
Address Offset: 18Ch
Default Value: 00h
Access: RO, R/W
Size: 8 bits

The operation of this register is detailed in the description for register C0DCLKDIS.

5.2.24 C1BNKARC—Channel 1 Bank Architecture

MMIO Range: MCHBAR
Address Offset: 18Eh
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

The operation of this register is detailed in the description for register C0BNKARC.

5.2.25 C1DRT0—Channel 1 DRAM Timing Register 0

MMIO Range:	MCHBAR
Address Offset:	190h
Default Value:	A96000E8h
Access:	RO, R/W
Size:	32 bits

The operation of this register is detailed in the description for register C0DRT0.

5.2.26 C1DRT1—Channel 1 DRAM Timing Register 1

MMIO Range:	MCHBAR
Address Offset:	194h
Default Value:	00006111h
Access:	RO, R/W
Size:	32 bits

The operation of this register is detailed in the description for register C0DRT1.

5.2.27 C1DRT2—Channel 1 DRAM Timing Register 2

PCI Device:	MCHBAR
Address Offset:	198h
Default Value:	000003FFh
Access:	RO, R/W
Size:	32 bits

The operation of this register is detailed in the description for register C0DRT2.

5.2.28 C1DRC0—Channel 1 DRAM Controller Mode 0

MMIO Range:	MCHBAR
Address Offset:	1A0h
Default Value:	40002801h
Access:	RO, R/W
Size:	32 bits

The operation of this register is detailed in the description for register C0DRC0.

5.2.29 C1DRC1—Channel 1 DRAM Controller Mode 1

MMIO Range:	MCHBAR
Address Offset:	1A4h
Default Value:	00000000h
Access:	RO, R/W
Size:	16 bits

The operation of this register is detailed in the description for register C0DRC1.

5.2.30 C1DRC2––Channel 1 DRAM Controller Mode 2

PCI Device: MCHBAR
Address Offset: 1A8h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

The operation of this register is detailed in the description for register C0DRC2.

5.2.31 DCC—DRAM Channel Control

MMIO Range: MCHBAR
Address Offset: 200h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

This register controls how the DRAM channels work together. It affects how the CxDRB registers are interpreted and allows them to steer transactions to the correct channel.

Bit	Access & Default	Description
31:20		**Reserved**
19	R/W 0 b	**Initialization Complete (IC):** See register description in C0DRC0[29]
18:16	R/W 000 b	**Mode Select (SMS):** See register description in C0DRC0[6:4]
15:3		**Reserved**
2	R/W 0 b	**Single Channel Selector (SCS):** When in Single Channel mode, this is the populated channel. 0: Channel 0 (Default) 1: Channel 1 (Reserved)
1:0	R/W 00 b	**DRAM Addressing Mode Control (DAMC):** 00: Single Channel 01: Dual Channel Asymmetric 10: Dual Channel Symmetric 11: Reserved

5.2.32 Device #0 MCHBAR Clock Controls

Table 5-1. Device #0 MCHBAR Clock/Thermal Sensor Controls

Address Offset (h)	Register Symbol	Register Name	Default Value	Access
C00-C03h	CLKCFG	GMCH Clock Configuration	00000000h	RO, R/W
C04-CEAh		***Reserved***		

5.2.33 CLKCFG—Clocking Configuration

PCI Device: MCHBAR
Address Offset: C00h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

These register bits are used for setting and changing DDR frequency, initializing GMCH memory clocks.

Bit	Access & Default	Description
31:29	R/W 0 b	**Reserved**
29:17	R/W 0000h	**Reserved**.
16	R/W 0 b	**Memory Core Clock control** 0 = DDR333, DDR400 (Default) (DDR533 @ Vcc = 1.5 V) 1 = DDR533 (for Intel® Pentium® M processor 90 nm, 2 MB L2 Cache, 533 MHz FSB support at Vcc =1.05 V) Please refer to the Mobile Intel® 915 Express Chipset Family BIOS Spec for details on programming the DDR ***PLL VCO Change Sequence.***
15:7	R/W 0 b	**Reserved**
6:4	RW strap dependent	**Memory Frequency Select.**
3	RO 0 b	**Reserved**
2:0	RO	**Reserved**

5.2.34 CPCTL—CPunit Control

PCI Device: MCHBAR
Address Offset: C16h
Size: 16 bits

Bit	Access & Default	Descriptions
15		Reserved

Bit	Access & Default	Descriptions
14	R/W/S 0 b	**MCHBAR register warm reset control** 0: All MCHBAR registers in the GMCH are reset to their default values upon RSTIN# assertion initiated by a “warm reset” 1: MCHBAR registers in the GMCH are NOT reset to defaults on a warm reset assertion; .
13:0		Reserved.

5.3 Device #0 MCHBAR ACPI Power Management Controls

5.3.1 PMSLFRFC—Dram Self Refresh Control

PCI Device: MCHBAR
Address Offset: F08h
Size: 16 bits

Bit	Access & Default	Description
15	RO 0 b	**Reserved**
14:13	R/W 00 b	**Reserved**
12:7	RO 000000 b	**Reserved**
6:4	R/W 000 b	**Self-refresh CPU State Dependency** Defines when self-refresh is allowed based on the CPU’s ACPI C state. This field only defines the CPU state conditions that must be met to use dynamic self-refresh. 000 = Not allowed in C0, C1, C2, C3, or C4 001 = Reserved 010 = Reserved 011 = Reserved 100 = Reserved 101 = Reserved 110 = Allowed in C3 and C4 only 111 = Reserved
3:0	R/W 0 h	**Reserved**

5.3.2 DSDLLPDC—Dram Slave DLL Power Down Control

PCI Device: MCHBAR
Address Offset: F0Ah
Size: 16 bits

Bit	Access & Default	Description
15	RO 0 b	**Reserved**
14:13	R/W 00 b	**Reserved**
12:7	RO 000000 b	**Reserved**
6:4	R/W 000 b	**Slave DLL Power-down CPU State Dependency** Defines when slave DLL power down is allowed based on the CPU's ACPI C state. This field only defines the CPU state conditions that must be met to use dynamic slave DLL power down. 000 = Not allowed in C0, C1, C2, C3, or C4 001 = Reserved 010 = Reserved 011 = Reserved 100 = Reserved 101 = Reserved 110 = Allowed in C3 and C4 only 111 = Reserved
3:0	R/W 0 h	**Reserved**

5.3.3 DMDLLPDC—Dram Master DLL Power Down Control

PCI Device: MCHBAR
Address Offset: F0Ch
Size: 16 bits

Bit	Access & Default	Description
15	RO 0 b	**Reserved**
14:13	R/W 00 b	**Reserved**
12:7	RO 000000 b	**Reserved**
6:4	R/W 000 b	**Master DLL Power-down CPU State Dependency** Defines when master DLL power-down is allowed based on the CPU's ACPI C state. This field only defines the CPU state conditions that must be met to use dynamic master DLL power-down. 000 = Not allowed in C0, C1, C2, C3, or C4 001 = Reserved 010 = Reserved 011 = Reserved 100 = Reserved 101 = Reserved 110 = Allowed in C3 and C4 only 111 = Reserved
3:0	R/W 0 h	**Reserved**

5.3.4 PMCFG—Power Management Configuration

PCI Device: MCHBAR
Address Offset: F10h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

Bit	Access & Default	Description
31	R/W 0 b	**Reserved**
30	R/W 0 b	**Reserved**
29:5	RO 0000000 h	**Reserved**
4	R/W 0 b	**Enhanced Power Management Features Enable** 0 = Legacy power management mode 1 = Enhanced power management
3	R/W 0 b	**Enhanced Power Management Snoop-detect Behavior** 0 = Snoop detection causes a request to the ICH6 for C2 1 = Snoop detection causes a request to the ICH6 for C0 Recommended setting = 0
2	R/W 0 b	**Reserved**
1:0	R/W 00 b	**Enhanced Power Management Mode** **00** = All enhanced power management functions allowed (Default) **01** = Disable the C2 to C3 transition. **Never go past C2**. **10** = Disable the C3 to C4 transition. **Never go past C3**. **11** = Reserved Recommended Setting = 00 Field is ignored if the Enhanced Power Management Feature Enable bit = 0

5.3.5 PMSTS—Power Management Status

PCI Device: MCHBAR
Address Offset: F14h
Default Value: 00000000h
Access: RO, R/WC
Size: 32 bits

This register is Reset by PWROK only.

Bit	Access & Default	Description
31:2	RO 00000000 h	**Reserved**
1	R/WC 0 b	**Channel 1 (B) in Self-refresh** Set by power management hardware after Channel 1 is placed in self refresh as a result of a Power State or a Reset Warn sequence, Cleared by Power management hardware before starting Channel 1 self refresh exit sequence initiated by a power management exit. Cleared by the Bios by writing a 1 in a warm reset (Reset# asserted while pwrok is asserted) exit sequence. 0 = Channel 1 not guaranteed to be in self-refresh. 1 = Channel 1 in Self-Refresh.
0	R/WC 0 b	**Channel 0 (A)in Self-refresh** Set by power management hardware after Channel 0 is placed in self refresh as a result of a Power State or a Reset Warn sequence, Cleared by Power management hardware before starting Channel 0 self refresh exit sequence initiated by a power management exit. Cleared by the Bios by writing a 1 in a warm reset (Reset# asserted while pwrok is asserted) exit sequence. 0 = Channel 0 not guaranteed to be in self refresh. 1 = Channel 0 in Self Refresh.

5.3.6 DMICC—DMI Countdown Control

MMIO Range: DMIBAR
Address Offset: 208h
Size: 32 bits

PCI Express configuration and control of various time related parameters that are not required by the PCI Express spec.

Bit	Access & Default	Description
31:24	R/W 00 h	**Reserved**
23:22	RO 0 h	**Reserved**
21	R/W 0 b	**Aggressive L0s Entry Enable** Once this bit is set, PCI Express Initialization unit will use aggressive L0s entry policy where 1/4th of the normally waited IDLE time is required 0 : Initialization Unit waits for "#FTS_required *4ns" of IDLE time to initiate the transition from L0 to L0s 1: Initialization Unit waits for "#FTS_required *4ns / 4" of IDLE time to initiate the transition from L0 to L0s *Note : These bits can be updated by BIOS during run time*
20:19	RO 00 b	**Reserved**
18:11	R/W 0F h	**Reserved**
10:0	R/W 4B0 h	**Reserved**

5.4 DMI RCRB

This section describes the mapped registers for the DMI. The DMIBAR register, described in Section 4.1.15 provides the base address for these registers.

This Root Complex Register Block (RCRB) controls the GMCH-ICH6-M serial interconnect that is based on the PCI Express 1.0 specification. An RCRB is required for configuration and control of elements that are located internal to a root complex that are not directly associated with a PCI Express device. The base address of this space is programmed in DMIBAR in device #0 config space.

Note: All RCRB register spaces needs to remain organized as they are here. The VC capabilities (or at least the first PCI Express Extended Capability) must begin at the 0h offset of the 4K area pointed to by the associated BAR. This is a PCI Express 1.0 specification requirement.

5.4.1 DMI Register Summary

Table 5-2. DMI Register Summary Table

Address Offset (h)	Register Symbol	Register Name	Default Value:	Access:
000-003h	DMIVCECH	DMI Virtual Channel Enhanced Capability Header	04010002h	RO
004-007h	DMIPVCCAP1	DMI Port VC Capability Register 1	00000001h	RO, R/WO
008-00Bh	DMIPVCCAP2	DMI Port VC Capability Register 2	00000001h	RO
00C-00Dh	DMIPVCCTL	DMI Port VC Control	0000h	RO, R/W
00E-00Fh		***Reserved***		
010-013h	DMIVC0RCAP	DMI VC0 Resource Capability	00000001h	RO
014-017h	DMIVC0RCTL0	DMI VC0 Resource Control	800000FFh	RO, R/W
018-019h		***Reserved***		
01A-01Bh	DMIVC0RSTS	DMI VC0 Resource Status	0002h	RO
01C-01Fh	DMIVC1RCAP	DMI VC1 Resource Capability	00010001h	RO
020-023h	DMIVC1RCTL1	DMI VC1 Resource Control	01000000h	RO, R/W
024-025h		***Reserved***		
026-027h	DMIVC1RSTS	DMI VC1 Resource Status	0002h	RO
028-03Fh		***Reserved***		
040-083h		***Reserved***		
084-087h	DMILCAP	DMI Link Capabilities	00002689h	RO
088-089h	DMILCTL	DMI Link Control	0000h	RO, R/W
08A-08Bh	DMILSTS	DMI Link Status	0001h	RO
08C-FFFh		***Reserved***		

5.4.2 DMIVCECH—DMI Virtual Channel Enhanced Capability Header

MMIO Range: DMIBAR
Address Offset: 000h
Default Value: 04010002h
Access: RO
Size: 32 bits

Indicates DMI Virtual Channel capabilities.

Bit	Access & Default	Description
31:20	RO 040 h	**Pointer to Next Capability** This field contains the offset to the next item in the list.
19:16	RO 1 h	**PCI Express Virtual Channel Capability Version** This field indicate compliances with the version 1 capability.
15:0	RO 0002 h	**Extended Capability ID** Value of 0002 h indicates this is the Virtual Channel capability item.

5.4.3 DMIPVCCAP1—DMI Port VC Capability Register 1

MMIO Range: DMIBAR
Address Offset: 004h
Default Value: 00000001h
Access: RO, R/WO
Size: 32 bits

Describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access & Default	Description
31:7		**Reserved**
11:10	RO 00 b	**Port Arbitration Table Entry Size (PATS):** This field indicates the size of the port arbitration table is 4 bits (to allow up to 8 ports)
9:8	RO 00 b	**Reference Clock (RC)** Fixed at 10ns.
7		**Reserved**
6:4	RO 000 b	**Low Priority Extended VC Count** Indicates that there are no additional VCs of low priority with extended capabilities.
3	RO 0 b	**Reserved**
2:0	R/WO 001 b	**Extended VC Count** Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device.

5.4.4 DMIPVCCAP2—DMI Port VC Capability Register 2

MMIO Range: DMIBAR
Address Offset: 008h
Default Value: 00000001h
Access: RO
Size: 32 bits

Describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access & Default	Description
31:24	RO 00 h	**VC Arbitration Table Offset (ATO)** Indicates that no table is present for VC arbitration since it is fixed.
23:8		**Reserved**
7:0	RO 01 h	**VC Arbitration Capability** Indicates that the VC arbitration is fixed in the root complex. VC1 is the highest priority and VC0 is the lowest priority.

5.4.5 DMIPVCCTL—DMI Port VC Control

MMIO Range: DMIBAR
Address Offset: 00Ch
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15:4		**Reserved**
3:1	R/W 000 b	**VC Arbitration Select** Indicates which VC should be programmed in the VC arbitration table. The root complex takes no action on the setting of this field since there is no arbitration table.
0	RO 0 b	**Load VC Arbitration Table (LAT)** Indicates that the table programmed should be loaded into the VC arbitration table. This bit is defined as read/write with always returning 0 on reads.

5.4.6 DMIVC0RCAP—DMI VC0 Resource Capability

MMIO Range: DMIBAR
Address Offset: 010h
Default Value: 00000001h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:24	RO 00 h	**Port Arbitration Table Offset (AT)** This VC implements no port arbitration table since the arbitration is fixed.
23		**Reserved**
22:16	RO 00 h	**Maximum Time Slots (MTS)** This VC implements fixed arbitration, and therefore this field is not used.
15	RO 0 b	**Reject Snoop Transactions** This VC must be able to take snoopable transactions.
14	RO 0 h	**Advanced Packet Switching (APS):** This VC is capable of all transactions, not just advanced packet switching transactions.
13:8		**Reserved**
7:0	RO 01 h	**Port Arbitration Capability** Having only bit 0 set indicates that the only supported arbitration scheme for this VC is non-configurable hardware-fixed.

5.4.7 DMIVC0RCTL0—DMI VC0 Resource Control

MMIO Range: DMIBAR
Address Offset: 014h
Default Value: 800000FFh
Access: RO, R/W
Size: 32 bits

Controls the resources associated with PCI Express Virtual Channel 0.

Bit	Access & Default	Description
31	RO 1 b	**Virtual Channel 0 Enable** Enables the VC when set. Disables the VC when cleared.
30:27		**Reserved**
26:24	RO 000 b	**Virtual Channel 0 ID** Indicates the ID used for this virtual channel
23:20		**Reserved**
19:17	R/W 0 h	**Port Arbitration Select** Indicates which port table is being programmed. The root complex takes no action on this setting since the arbitration is fixed and there is no arbitration for this virtual channel
16	RO 0 b	**Load Port Arbitration Table (LAT):** The root complex does not implement an arbitration table for this virtual channel.
15:8		**Reserved**
7:1	R/W 1111111 b	**Transaction Class / Virtual Channel Map (TVM)** This field indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel.
0		**Reserved**

5.4.8 DMIVC0RSTS—DMI VC0 Resource Status

MMIO Range: DMIBAR
Address Offset: 01Ah
Default Value: 0002h
Access: RO
Size: 16 bits

Reports the Virtual Channel specific status.

Bit	Access & Default	Description
15:2		**Reserved**
1	RO 1 b	**VC Negotiation Pending:** 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling).
0	RO 0 b	**Port Arbitration Tables Status (ATS):** There is no port arbitration table for this VC, so this bit is reserved at 0.

5.4.9 DMIVC1RCAP—DMI VC1 Resource Capability

MMIO Range: DMIBAR
Address Offset: 01Ch
Default Value: 00010001h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:24	RO 00 h	**Port Arbitration Table Offset (AT)** Indicates the location of the port arbitration table in the root complex. A value of 3h indicates the table is at offset 30h.
23		**Reserved**
22:16	RO 00 h	**Maximum Time Slots (MTS)** This value is updated by platform BIOS based upon the determination of the number of time slots available in the platform.
15	RO 1 b	**Reject Snoop Transactions (RTS):** All snoopable transactions on VC1 are rejected. This VC is for isochronous transfers only.
14	RO 0 b	**Advanced Packet Switching (APS)** This VC is capable of all transactions, not just advanced packet switching transactions.
13:8		**Reserved**
7:0	RO 01 h	**Port Arbitration Capability** This field indicates the port arbitration capability is time-based WRR of 128 phases.

5.4.10 DMIVC1RCTL1—DMI VC1 Resource Control

MMIO Range: DMIBAR
Address Offset: 020h
Default Value: 01000000h
Access: RO, R/W
Size: 32 bits

Controls the resources associated with PCI Express Virtual Channel 1.

Bit	Access & Default	Description
31	R/W 0 b	**Virtual Channel 1 Enable** 0: Virtual Channel is disabled. 1: Virtual Channel is enabled.
30:27		**Reserved**
26:24	R/W 001 b	**Virtual Channel 1 ID** Assigns a VC ID to the VC resource. This field can not be modified when the VC is already enabled.
23:20		**Reserved**
19:17	R/W 000 b	**Port Arbitration Select** This field indicates which port table is being programmed. The only permissible value of this field is 4h for the time-based WRR entries.
16:8		**Reserved**
7:1	R/W 00h	**Transaction Class / Virtual Channel Map (TVM)** The Field indicates which transaction classes are mapped to this virtual channel. When a bit is set, this transaction class is mapped to the virtual channel.
0		**Reserved**

5.4.11 DMIVC1RSTS—DMI VC1 Resource Status

MMIO Range: DMIBAR
Address Offset: 026h
Default Value: 0002h
Access: RO
Size: 16 bits

Reports the Virtual Channel specific status

Bit	Access & Default	Description
15:2		**Reserved**
1	RO 1 b	**VC1 Negotiation Pending** 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling).
0		**Reserved**

5.4.12 DMILCAP—DMI Link Capabilities

MMIO Range: DMIBAR
Address Offset: 084h
Default Value: 00012C41h
Access: RO, R/WO
Size: 32 bits

Indicates DMI specific capabilities.

Bit	Access & Default	Description
31:18		**Reserved**
17:15	R/WO 010 b	**L1 Exit Latency** L1 not supported on DMI
14:12	R/WO 010 b	**L0s Exit Latency** Indicates the length of time this Port requires to complete the transition from L0s to L0. The value 010 b indicates the range of 128 ns to less than 256 ns.
11:10	RO 11 b	**Active State Link PM Support (APMS)** This field indicates that L0s is supported on DMI. Note: ICH6 does not support L1 entry on DMI interface
9:4	RO 000100 b	**Max Link Width (MLW)** This field indicates the maximum link width is either x2 (2h) or X4. (4h)
3:0	RO 0001 b	**Maximum Link Speed (MLS)** This field indicates the link speed is 2.5 Gb/s.

5.4.13 DMILCTL—DMI Link Control

MMIO Range: DMIBAR
Address Offset: 088h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Allows control of DMI.

Bit	Access & Default	Description
15:8	RO 00 h	**Reserved**
7	R/W 0 h	**Extended Synch** 0: Standard Fast Training Sequence (FTS). 1 = Forces extended transmission of FTS ordered sets when exiting L0s prior to entering L0 and extra TS1 sequences at exit from L1 to entering L0.
6:2	00000 b	**Reserved**
1:0	R/W 00 b	**Active State PM** Controls the level of active state power management supported on the given link. 00: Disabled 01: L0s Entry Enabled 10: Reserved 11: Reserved

5.4.14 DMILSTS—DMI Link Status

MMIO Range: DMIBAR
Address Offset: 08Ah
Default Value: 0001h
Access: RO
Size: 16 bits

Indicates DMI status.

Bit	Access & Default	Description
15:10	RO 000000 b	**Reserved**
9:4	RO 00 h	**Negotiated Width** Indicates negotiated link width 00h: Reserved 01h: Reserved 02h: X2 04h: X4 All other encodings are reserved.
3:0	RO 1 h	**Negotiated Speed** Indicates negotiated link speed. 1h: 2.5 Gb/s All other encodings are reserved.

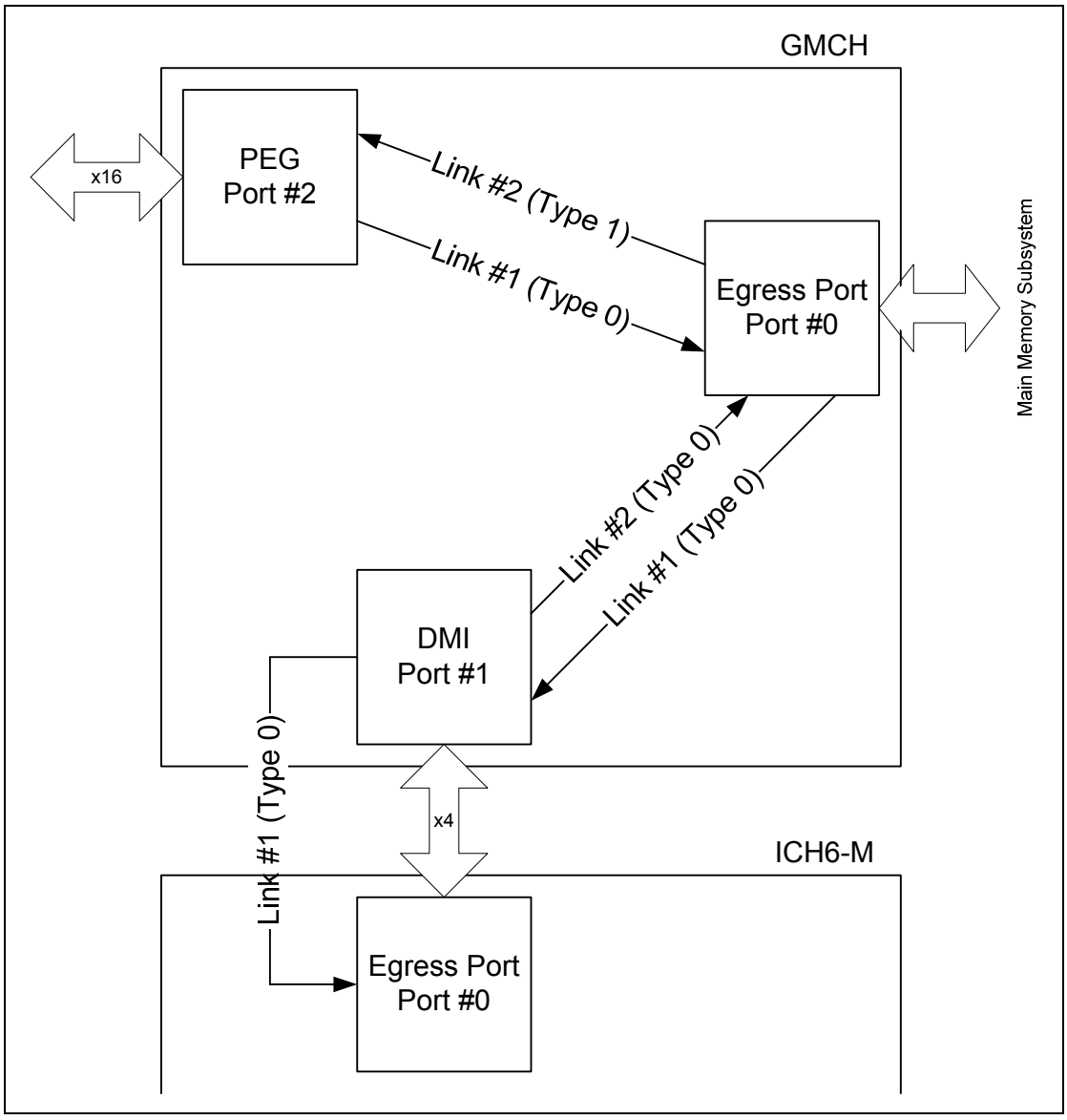
5.4.15 Egress Port (EP) RCRB

This Root Complex Register Block (RCRB) controls the port arbitration that is based on the PCI Express 1.0 specification. Port arbitration is done for all PCI Express based isochronous requests (always on Virtual Channel 1) before being submitted to the main memory arbiter. The base address of this space is programmed in EPBAR in device #0 config space.

5.4.16 EP Register Summary

Address Offset (h)	Register Symbol	Register Name	Default Value	Access
000-043h		***Reserved***		
044-047h	EPESD	EP Element Self Description	00000201h	RO, RWO
048-04Fh		***Reserved***		
050-053h	EPLE1D	EP Link Entry 1 Description	01000000h	RO, R/WO
054-057h		***Reserved***		
058-05Fh	EPLE1A	EP Link Entry 1 Address	000…	RO, R/WO
060-063h	EPLE2D	EP Link Entry 2 Description	02000002h	RO, R/WO
064-067h		***Reserved***		
068-06Fh	EPLE2A	EP Link Entry 2 Address	000…	RO
070-FFFh		***Reserved***		

Figure 5-1. Link Declaration Topology



5.4.17 EPESD—EP Element Self Description

MMIO Range: EPBAR
Address Offset: 044h
Default Value: 00000201h
Access: RO, R/WO
Size: 32 bits

Provides information about the root complex element containing this Link Declaration Capability.

Bit	Access & Default	Description
31:24	RO 00 h	**Port Number. –** This field specifies the port number associated with this element with respect to the component that contains this element. Value of 00 h indicates to configuration software that this is the default egress port.
23:16	R/WO 00 h	**Component ID –** Identifies the physical component that contains this Root Complex Element. Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. The value only needs to be written in one of the mirrored fields and it will be reflected everywhere that it is mirrored.
15:8	RO 02 h	**Number of Link Entries –** Indicates the number of link entries following the Element Self Description. This field reports 2 (one each for PCI Express* Based Graphics and DMI).
7:0		**Reserved**

5.4.18 EPLE1D—EP Link Entry 1 Description

MMIO Range: EPBAR
Address Offset: 050h
Default Value: 01000000h
Access: RO, R/WO
Size: 32 bits

First part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
31:24	RO 01 h	**Target Port Number –** Specifies the port number associated with the element targeted by this link entry (DMI). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO 00 h	**Target Component ID –** Identifies the physical or logical component that is targeted by this link entry. A value of 0 is reserved; Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. The value only needs to be written in one of the mirrored fields and it will be reflected everywhere that it is mirrored.
15:2		**Reserved**
1	RO 0 b	**Link Type –** Indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	R/WO 0 b	**Link Valid** 0: Link Entry is not valid and will be ignored. 1: Link Entry specifies a valid link.

5.4.19 EPLE1A—EP Link Entry 1 Address

MMIO Range: EPBAR
Address Offset: 058h
Default Value: 0000000000000000h
Access: RO, R/WO
Size: 64 bits

Second part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
63:32		**Reserved**
31:12	R/WO 0 0000 h	**Link Address** Memory mapped base address of the RCRB that is the target element (DMI) for this link entry.
11:0		**Reserved**

5.4.20 EPLE2D—EP Link Entry 2 Description

MMIO Range: EPBAR
Address Offset: 060h
Default Value: 0200002h
Access: RO, R/WO
Size: 32 bits

First part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
31:24	RO 02 h	**Target Port Number** Specifies the port number associated with the element targeted by this link entry (PEG). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO 00 h	**Target Component ID** Identifies the physical or logical component that is targeted by this link entry. A value of 0 is reserved; Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. The value only needs to be written in one of the mirrored fields and it will be reflected everywhere that it is mirrored.
15:2		**Reserved**
1	RO 1 b	**Link Type** Indicates that the link points to configuration space of the integrated device which controls the x16 root port. The link address specifies the configuration address (segment, bus, device, function) of the target root port.
0	R/WO 0 b	**Link Valid** 0: Link Entry is not valid and will be ignored. 1: Link Entry specifies a valid link.

5.4.21 E2A—EP Link Entry 2 Address

MMIO Range: EPBAR
Address Offset: 068h
Default Value: 0000000000008000h
Access: RO
Size: 64 bits

Second part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
63:28		**Reserved**
27:20	RO 00 h	**Bus Number**
19:15	RO 0 0001 b	**Device Number** Target for this link is PCI Express x16 port (Device 1).
14:12	RO 000 b	**Function Number**
11:0		**Reserved**

§



6 PCI Express Graphics Device 1 Configuration Registers (D1:F0)

Note: Excludes Mobile Intel® 915GMS, 910GML and 910GMLE Express Chipsets.

Device #1 contains the controls associated with the x16 root port that is the intended attach point for external graphics. It is typically referred to as PEG (PCI Express Graphics) port. It also functions as the virtual PCI-to-PCI Bridge that was previously associated with AGP.

Warning: When reading the PCI Express "conceptual" registers such as this, you may not get a valid value unless the register value is stable.

The PCI Express Specification defines two types of reserved bits:

- Reserved and Preserved: Reserved for future RW implementations; software must preserve value read for writes to bits.
- Reserved and Zero: Reserved for future R/WC/S implementations; software must use 0 for writes to bits.

Unless explicitly documented as Reserved and Zero, all bits marked as Reserved are part of the Reserved and Preserved type which has historically been the typical definition for Reserved.

Most (if not all) control bits in this device cannot be modified unless the link is down. Software is required to first disable the link, then program the registers, then re-enable the link (which will cause a full-retrain with the new settings).

Note: Register information for the PCI Express Based x16 Graphics Port is NOT relative to the Mobile Intel® 82915GMS, 82910GML and 82910GMLE Express Chipsets.

Note: Register information for the Integrated Graphics Device is NOT relative to the Mobile Intel 82915PM Express Chipset.

6.1 PEG Device 1 Configuration Register Summary

Table 6-1. PCI Express Graphics Port Configuration Register Summary

Register Offset (h)	Register Symbol	Register Name	Default Value	Access
00-01h	VID1	Vendor Identification	8086h	RO
02-03h	DID1	Device Identification	2591h	RO
04-05h	PCICMD1	PCI Command	0000h	RO, R/W
06-07h	PCISTS1	PCI Status	0010h	RO, R/WC
08h	RID1	Revision Identification	00h	RO
09-0Bh	CC1	Class Code	060400h	RO
0Ch	CL1	Cache Line Size	00h	R/W
0Dh		***Reserved***		
0Eh	HDR1	Header Type	01h	RO
0F-17h		***Reserved***		
18h	PBUSN1	Primary Bus Number	00h	RO
19h	SBUSN1	Secondary Bus Number	00h	R/W
1Ah	SUBUSN1	Subordinate Bus Number	00h	R/W
1Bh		***Reserved***		
1Ch	IOBASE1	I/O Base Address	F0h	RO,R/W
1Dh	IOLIMIT1	I/O Limit Address	00h	RO, R/W
1E-1Fh	SSTS1	Secondary Status	0000h	RO, R/WC
20-21h	MBASE1	Memory Base Address	FFF0h	RO, R/W
22-23h	MLIMIT1	Memory Limit Address	0000h	RO, R/W
24-25h	PMBASE1	Prefetchable Memory Base Address	FFF0h	RO, R/W
26-27h	PMLIMIT1	Prefetchable Memory Limit Address	0000h	RO, R/W
28-33h		***Reserved***		
34h	CAPPTR1	Capabilities Pointer	88h	RO
35-3Bh		***Reserved***		
3Ch	INTRLINE1	Interrupt Line	00h	R/W
3Dh	INTRPIN1	Interrupt Pin	01h	RO
3E-3Fh	BCTRL1	Bridge Control	0000h	RO, R/W
40-7Fh		***Reserved***		
80-83h	PM_CAP1	Power Management Capabilities	1902 / A001h	RO
84-87h	PM_CS1	Power Management Control/Status	00000000h	RO, R/W/S
88-8Bh	SS_CAPID	Subsystem ID and Vendor ID Capabilities	0000800Dh	RO
8C-8Fh	SS	Subsystem ID and Subsystem Vendor ID	00008086h	R/WO
90-91h	MSI_CAPID	Message Signaled Interrupts Capability ID	A005h	RO
92-93h	MC	Message Control	0000h	RO, R/W
94-97h	MA	Message Address	0000000h	RO, R/W
98-99h	MD	Message Data	0000h	R/W

Register Offset (h)	Register Symbol	Register Name	Default Value	Access
9A-9Fh		***Reserved***		
A0-A1h	PEG_CAPL	PCI Express Capability List	0010h	RO
A2-A3h	PEG_CAP	PCI Express Capabilities	0141h	RO
A4-A7h	DCAP	Device Capabilities	00000000h	RO
A8-A9h	DCTL	Device Control	0000h	RO, R/W
AA-ABh	DSTS	Device Status	0000h	RO, R/WC
AC-AFh	LCAP	Link Capabilities	02012801h	RO, R/WO
B0-B1h	LCTL	Link Control	0000h	RO, R/W
B2-B3h	LSTS	Link Status	1001h	RO
B4-B7H	SLOTCAP	Slot Capabilities	00000000h	RO, R/WO
B8-B9h	SLOTCTL	Slot Control	01C0h	RO, R/W
BA-BBh	SLOTSTS	Slot Status	0000h	RO, R/WC
BC-BDh	RCTL	Root Control	0000h	RO, R/W
BE-BFh		***Reserved***		
C0-C3h	RSTS	Root Status	00000000h	RO, R/W/C
C4-FFh		***Reserved***		
100-103h	VCECH	Virtual Channel Enhanced Capability Header	14010002h	RO
104-107h	PVCCAP1	Port VC Capability Register 1	00000001h	RO, R/WO
108-10Bh	PVCCAP2	Port VC Capability Register 2	00000000h	RO
10C-10Dh	PVCCTL	Port VC Control	0000h	RO, R/W
10E-10Fh		***Reserved***		
110-113h	VC0RCAP	VC0 Resource Capability	00000000h	RO
114-117h	VC0RCTL	VC0 Resource Control	800000FFh	FO, R/W
118-119h		***Reserved***		
11A-11Bh	VC0RSTS	VC0 Resource Status	0000h	RO
11C-11Fh	VC1RCAP	VC1 Resource Capability	00008000h	RO
120-123h	VC1RCTL	VC1 Resource Control	01000000h	RO, R/W
124-125h		***Reserved***		
126-127h	VC1RSTS	VC1 Resource Status	0000h	RO
128-13Fh		***Reserved***		
140-143h	RCLDECH	Root Complex Link Declaration Enhanced Capability Header	00010005h	RO
144-147h	ESD	Element Self Description	02000100h	RO, R/WO
148-14Fh		***Reserved***		
150-153h	LE1D	Link Entry 1 Description	00000000h	RO, R/WO
154-157h		***Reserved***		
158-15Fh	LE1A	Link Entry 1 Address	0000000000000000h	RO, R/WO
160-217h		***Reserved***		
218-21Fh	PEGSSTS	PCI Express Graphics Sequence Status	0000000000000FFFh	RO
220-2FFh		***Reserved***		



6.2 PEG Device 1 Configuration Register Details

6.2.1 VID1—Vendor Identification

PCI Device: 1
Address Offset: 00h
Default Value: 8086h
Access: RO
Size: 16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 8086 h	**Vendor Identification (VID1)** PCI standard identification for Intel.

6.2.2 DID1—Device Identification

PCI Device: 1
Address Offset: 02h
Default Value: 2591h
Access: RO
Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 2591h	**Device Identification Number (DID1)** Identifier assigned to the GMCH device #1 (virtual PCI-to-PCI bridge, PCI Express Graphics port). .

6.2.3 PCICMD1—PCI Command

PCI Device: 1
Address Offset: 04h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15:11		**Reserved.**
10	R/W 0 b	**INTA Assertion Disable** 0: This device is permitted to generate INTA interrupt messages. 1: This device is prevented from generating interrupt messages. Any INTA emulation interrupts already asserted must be deasserted when this bit is set. Only affects interrupts generated by the device (PCI INTA from a PME or Hot Plug event) controlled by this command register. It does not affect upstream MSI's, upstream PCI INTA-INTD assert and deassert messages.
9	RO 0 b	**Fast Back-to-Back Enable (FB2B)** Not Applicable or Implemented. Hardwired to 0.
8	R/W 0 b	**SERR Message Enable (SERRE1)** This bit is an enable bit for Device #1 SERR messaging. The GMCH communicates the SERRB condition by sending an SERR message to the ICH. This bit, when set, enables reporting of non-fatal and fatal errors to the Root Complex. Note that errors are reported if enabled either through this bit or through the PCI-Express specific bits in the Device Control Register 0: The SERR message is generated by the GMCH for Device #1 only under conditions enabled individually through the Device Control Register. 1: The GMCH is enabled to generate SERR messages which will be sent to the ICH for specific Device #1 error conditions that are individually enabled in the BCTRL1 register and for all non-fatal and fatal errors generated on the primary side of the virtual PCI to PCI-Express bridge (not those received by the secondary side). The error status is reported in the PCISTS1 register.
7		**Reserved.**
6	R/WO 0 b	**Parity Error Enable (PERRE)** Controls whether or not the Master Data Parity Error bit in the PCI Status register can bet set. 0: Master Data Parity Error bit in PCI Status register **cannot** be set. 1: Master Data Parity Error bit in PCI Status register **can** be set.
5	RO 0 b	**VGA Palette Snoop** Not Applicable or Implemented. Hardwired to 0.
4	RO 0 b	**Memory Write and Invalidate Enable (MWIE)** Not Applicable or Implemented. Hardwired to 0.
3	RO 0 b	**Special Cycle Enable (SCE)** Not Applicable or Implemented. Hardwired to 0.

Bit	Access & Default	Description
2	R/W 0 b	**Bus Master Enable (BME)** 0: This device is prevented from making memory or IO requests to its primary bus. Note that according to PCI Specification, as MSI interrupt messages are in-band memory writes, disabling the bus master enable bit prevents this device from generating MSI interrupt messages or passing them from its secondary bus to its primary bus. Upstream memory writes/reads, IO writes/reads, peer writes/reads, and MSI's will all be treated as illegal cycles. Writes are forwarded to memory address 0 with byte enables deasserted. Reads will be forwarded to memory address 0 and will return Unsupported Request status (or Master abort) in its completion packet. 1: This device is allowed to issue requests to its primary bus. Completions for previously issued memory read requests on the primary bus will be issued when the data is available. This bit does not affect forwarding of Completions from the primary interface to the secondary interface.
1	R/W 0 b	**Memory Access Enable (MAE)** 0: All of device #1's memory space is disabled. 1: Enable the Memory and Pre-fetchable memory address ranges defined in the MBASE1, MLIMIT1, PMBASE1, and PMLIMIT1 registers.
0	R/W 0 b	**IO Access Enable (IOAE)** 0: All of device #1's I/O space is disabled. 1: Enable the I/O address range defined in the IOBASE1, and IOLIMIT1 registers.

6.2.4 PCISTS1—PCI Status

PCI Device: 1
Address Offset: 06h
Default Value: 0010h
Access: RO, R/WC
Size: 16 bits

This register reports the occurrence of error conditions associated with primary side of the "virtual" Host-PCI Express bridge embedded within the GMCH.

Bit	Access & Default	Description
15	RO 0 b	**Detected Parity Error (DPE)** Hardwired to 0. Parity (generating poisoned TLPs) is not supported on the primary side of this device.
14	R/WC 0 b	**Signaled System Error (SSE)** This bit is set when this Device sends an SERR due to detecting an ERR_FATAL or ERR_NONFATAL condition and the SERR Enable bit in the Command register is 1. Both received (if enabled by BCTRL1[1]) and internally detected error messages do not affect this field.
13	RO 0 b	**Received Master Abort Status (RMAS)** Not Applicable or Implemented. Hardwired to 0. The concept of a master abort does not exist on primary side of this device.
12	RO 0 b	**Received Target Abort Status (RTAS)** Not Applicable or Implemented. Hardwired to 0. The concept of a target abort does not exist on primary side of this device.
11	RO 0 b	**Signaled Target Abort Status (STAS)** Not Applicable or Implemented. Hardwired to 0. The concept of a target abort does not exist on primary side of this device.
10:9	RO 00 b	**DEVSELB Timing (DEVT)** This device is not the subtractively decoded device on bus 0. This bit field is therefore hardwired to 00 to indicate that the device uses the fastest possible decode.
8	RO 0 b	**Master Data Parity Error (PMDPE)** Because the primary side of the PCI Express* x16 Graphics Interface's virtual P2P bridge is integrated with the MCH functionality there is no scenario where this bit will get set. Because hardware will never set this bit, it is impossible for software to have an opportunity to clear this bit or otherwise test that it is implemented. The PCI specification defines it as a R/WC, but for our implementation an RO definition behaves the same way and will meet all Microsoft testing requirements. This bit can only be set when the Parity Error Enable bit in the PCI Command register is set.
7	RO 0 b	**Fast Back-to-Back (FB2B)** Not Applicable or Implemented. Hardwired to 0.
6		**Reserved.**
5	RO 0 b	**66/60 MHz capability (CAP66)** Not Applicable or Implemented. Hardwired to 0.
4	RO 1 b	**Capabilities List** Indicates that a capabilities list is present. Hardwired to 1.
3	RO 0 b	**INTA Status** Indicates that an interrupt message is pending internally to the device. Only PME and Hot Plug sources feed into this status bit (not PCI INTA-INTD assert and deassert messages). The INTA Assertion Disable bit, PCICMD1[10], has no effect on this bit.
2:0		**Reserved.**

6.2.5 RID1—Revision Identification

PCI Device: 1
Address Offset: 08h
Default Value: 00h
Access: RO
Size: 8 bits

This register contains the revision number of the GMCH device #1. These bits are read only and writes to this register have no effect.

Bit	Access & Default	Description
7:0	RO 00 h	**Revision Identification Number (RID1)** Indicates the number of times that this device in this component has been "stepped" through the manufacturing process. It is always the same as the RID values in all other devices in this component.

6.2.6 CC1—Class Code

PCI Device: 1
Address Offset: 09h
Default Value: 060400h
Access: RO
Size: 24 bits

This register identifies the basic function of the device, a more specific sub-class, and a register-specific programming interface.

Bit	Access & Default	Description
23:16	RO 06 h	**Base Class Code (BCC)** Indicates the base class code for this device. This code has the value 06h, indicating a Bridge device.
15:8	RO 04 h	**Sub-Class Code (SUBCC)** Indicates the sub-class code for this device. The code is 04h indicating a PCI to PCI Bridge.
7:0	RO 00 h	**Programming Interface (PI)** Indicates the programming interface of this device. This value does not specify a particular register set layout and provides no practical use for this device.

6.2.7 CL1—Cache Line Size

PCI Device: 1
Address Offset: 0Ch
Default Value: 00h
Access: R/W
Size: 8 bits

Bit	Access & Default	Description
7:0	R/W 00 h	**Cache Line Size (Scratch pad)** Implemented by PCI Express devices as a read-write field for legacy compatibility purposes but has no impact on any PCI Express device functionality.

6.2.8 HDR1—Header Type

PCI Device: 1
Address Offset: 0Eh
Default Value: 01h
Access: RO
Size: 8 bits

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Access & Default	Description
7:0	RO 01 h	**Header Type Register (HDR)** Returns 01 to indicate that this is a single function device with bridge header layout.

6.2.9 PBUSN1—Primary Bus Number

PCI Device: 1
Address Offset: 18h
Default Value: 00h
Access: RO
Size: 8 bits

This register identifies that this “virtual” Host-PCI Express bridge is connected to PCI bus #0.

Bit	Access & Default	Description
7:0	RO 00 h	**Primary Bus Number (BUSN)** Configuration software typically programs this field with the number of the bus on the primary side of the bridge. Since device #1 is an internal device and its primary bus is always 0, these bits are read only and are hardwired to 0.

6.2.10 SBUSN1—Secondary Bus Number

PCI Device: 1
Address Offset: 19h
Default Value: 00h
Access: R/W
Size: 8 bits

This register identifies the bus number assigned to the second bus side of the "virtual" bridge i.e. to PCI Express Graphics. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI Express Graphics.

Bit	Access & Default	Description
7:0	R/W 00 h	**Secondary Bus Number (BUSN)** This field is programmed by configuration software with the bus number assigned to PCI Express Graphics.

6.2.11 SUBUSN1—Subordinate Bus Number

PCI Device: 1
Address Offset: 1Ah
Default Value: 00h
Access: R/W
Size: 8 bits

This register identifies the subordinate bus (if any) that resides at the level below PCI Express Graphics. This number is programmed by the PCI configuration software to allow mapping of configuration cycles to PCI Express Graphics.

Bit	Access & Default	Description
7:0	R/W 00 h	**Subordinate Bus Number (BUSN)** This register is programmed by configuration software with the number of the highest subordinate bus that lies behind the device #1 bridge. When only a single PCI device resides on the PCI Express Graphics segment, this register will contain the same value as the SBUSN1 register.

6.2.12 IOBASE1—I/O Base Address

PCI Device: 1
Address Offset: 1Ch
Default Value: F0h
Access: RO, R/W
Size: 8 bits

This register controls the CPU to PCI Express Graphics I/O access routing based on the following formula:

IO_BASE=< address =<IO_LIMIT

Only upper 4 bits are programmable. For the purpose of address decode address bits A[11:0] are treated as 0. Thus the bottom of the defined I/O address range will be aligned to a 4-kB boundary.

Bit	Access & Default	Description
7:4	R/W F h	**I/O Address Base (IOBASE)** Corresponds to A[15:12] of the I/O addresses passed by bridge 1 to PCI Express-Graphics interface. BIOS must not set this register to 00h otherwise 0CF8h/0CFCh accesses will be forwarded to the PCI Express hierarchy associated with this device.
3:0	RO 0 h	**Reserved.**

6.2.13 IOLIMIT1—I/O Limit Address

PCI Device: 1
Address Offset: 1Dh
Default Value: 00h
Access: RO, R/W
Size: 8 bits

This register controls the CPU to PCI Express Graphics I/O access routing based on the following formula:

IO_BASE=< address =<IO_LIMIT

Only upper 4 bits are programmable. For the purpose of address decode address bits A[11:0] are assumed to be FFFh. Thus, the top of the defined I/O address range will be at the top of a 4-kB aligned address block.

Bit	Access & Default	Description
7:4	R/W 0 h	**I/O Address Limit (IOLIMIT)** Corresponds to A[15:12] of the I/O address limit of device #1. Devices between this upper limit and IOBASE1 will be passed to the PCI Express hierarchy associated with this device.
3:0	RO 0 h	**Reserved.**

6.2.14 SSTS1—Secondary Status

PCI Device: 1
Address Offset: 1Eh
Default Value: 0000h
Access: RO, R/WC
Size: 16 bits

SSTS1 is a 16-bit status register that reports the occurrence of error conditions associated with secondary side (i.e. PCI Express Graphics side) of the "virtual" PCI-PCI Bridge embedded within GMCH.

Bit	Access & Default	Description
15		**Reserved.**
14	R/WC 0 b	**Received System Error (RSE)** This bit is set when the secondary side sends an ERR_FATAL or ERR_NONFATAL message due to an error detected by the secondary side, and the SERR Enable bit in the Bridge Control register is 1.
13	R/WC 0 b	**Received Master Abort (RMA)** This bit is set when the Secondary Side for Type 1 Configuration Space Header Device (for requests initiated by the Type 1 Header Device itself) receives a Completion with **Unsupported Request** Completion Status.
12	R/WC 0 b	**Received Target Abort (RTA)** This bit is set when the Secondary Side for Type 1 Configuration Space Header Device (for requests initiated by the Type 1 Header Device itself) receives a Completion with **Completer Abort** Completion Status.
11	RO 0 b	**Signaled Target Abort (STA)** Not Applicable or Implemented. Hardwired to 0. The GMCH does not generate Target Aborts (the GMCH will never complete a request using the Completer Abort Completion status).
10:9	RO 00 b	**DEVSELB Timing (DEVT)** Not Applicable or Implemented. Hardwired to 0.
8		**Reserved**
7	RO 0 b	**Fast Back-to-Back (FB2B)** Hardwired to 0.
6		**Reserved.**
5	RO 0 b	**66/60 MHz capability (CAP66)** Hardwired to 0.
4:0		**Reserved.**

6.2.15 MBASE1—Memory Base Address

PCI Device: 1
Address Offset: 20h
Default Value: FFF0h
Access: RO, R/W
Size: 16 bits

This register controls the CPU to PCI Express Graphics non-prefetchable memory access routing based on the following formula:

MEMORY_BASE=< address =<MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32 bit address. The bottom 4 bits of this register are read-only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bit	Access & Default	Description
15:4	R/W FFF h	**Memory Address Base (MBASE)** Corresponds to A[31:20] of the lower limit of the memory range that will be passed to PCI Express Graphics.
3:0	RO 0 h	**Reserved.**

6.2.16 MLIMIT1—Memory Limit Address

PCI Device: 1
Address Offset: 22h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register controls the CPU to PCI Express Graphics non-prefetchable memory access routing based on the following formula:

MEMORY_BASE=< address =<MEMORY_LIMIT

The upper 12 bits of the register are read/write and correspond to the upper 12 address bits A[31:20] of the 32 bit address. The bottom 4 bits of this register are read-only and return zeroes when read. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1MB aligned memory block.

Note: Memory range covered by MBASE and MLIMIT registers are used to map non-prefetchable PCI Express Graphics address ranges (typically where control/status memory-mapped I/O data structures of the graphics controller will reside) and PMBASE and PMLIMIT are used to map prefetchable address ranges (typically graphics local memory). This segregation allows application of USWC space attribute to be performed in a true plug-and-play manner to the prefetchable address range for improved CPU-PCI Express memory access performance.

Note also that configuration software is responsible for programming all address range registers (prefetchable, non-prefetchable) with the values that provide exclusive address ranges i.e. prevent overlap with each other and/or with the ranges covered with the main memory. There is no provision in the GMCH hardware to enforce prevention of overlap and operations of the system in the case of overlap are not guaranteed.

Bit	Access & Default	Description
15:4	R/W 000 h	**Memory Address Limit (MLIMIT)** Corresponds to A[31:20] of the upper limit of the address range passed to PCI Express Graphics.
3:0	RO 0 h	**Reserved**

6.2.17 PMBASE1—Prefetchable Memory Base Address

PCI Device: 1
Address Offset: 24h
Default Value: FFF0h
Access: RO, R/W
Size: 16 bits

This register in conjunction with the corresponding Upper Base Address register controls the CPU to PCI Express Graphics prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE =< address =< PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Base Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bit	Access & Default	Description
15:4	R/W FFF h	**Prefetchable Memory Base Address (MBASE)** Corresponds to A[31:20] of the lower limit of the memory range that will be passed to PCI Express Graphics.
3:0	RO 0 h	**64-bit Address Support** Indicates the bridge supports only 32 bit addresses.

6.2.18 PMLIMIT1—Prefetchable Memory Limit Address

PCI Device: 1
Address Offset: 26h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register in conjunction with the corresponding Upper Limit Address register controls the CPU to PCI Express Graphics prefetchable memory access routing based on the following formula:

PREFETCHABLE_MEMORY_BASE =< address =< PREFETCHABLE_MEMORY_LIMIT

The upper 12 bits of this register are read/write and correspond to address bits A[31:20] of the 40-bit address. The lower 8 bits of the Upper Limit Address register are read/write and correspond to address bits A[39:32] of the 40-bit address. This register must be initialized by the configuration software. For the purpose of address decode address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block. Note that prefetchable memory range is supported to allow segregation by the configuration software between the memory ranges that must be defined as UC and the ones that can be designated as a USWC (i.e. prefetchable) from the CPU perspective.

Bit	Access & Default	Description
15:4	R/W 000 h	**Prefetchable Memory Address Limit (PMLIMIT)** Corresponds to A[31:20] of the upper limit of the address range passed to PCI Express Graphics.
3:0	RO 0 h	**64-bit Address Support** Indicates the bridge supports only 32 bit addresses.

6.2.19 CAPPTR1—Capabilities Pointer

PCI Device: 1
Address Offset: 34h
Default Value: 88h
Access: RO
Size: 8 bits

The capabilities pointer provides the address offset to the location of the first entry in this device's linked list of capabilities.

Bit	Access & Default	Description
7:0	RO 88h	**First Capability (CAPPTR1)** The first capability in the list is the Subsystem ID and Subsystem Vendor ID Capability.

6.2.20 INTRLINE1—Interrupt Line

PCI Device: 1
Address Offset: 3Ch
Default Value: 00h
Access: R/W
Size: 8 bits

This register contains interrupt line routing information. The device itself does not use this value, rather it is used by device drivers and operating systems to determine priority and vector information.

Bit	Access & Default	Description
7:0	R/W 00 h	**Interrupt Connection.** Used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates which input of the system interrupt controller this device's interrupt pin is connected to.

6.2.21 INTRPIN1—Interrupt Pin

PCI Device: 1
Address Offset: 3Dh
Default Value: 01h
Access: RO
Size: 8 bits

This register specifies which interrupt pin this device uses.

Bit	Access & Default	Description
7:0	RO 01 h	**Interrupt Pin.** As a single function device, the PCI Express device specifies INTA as its interrupt pin. 01h=INTA.

6.2.22 BCTRL1—Bridge Control

PCI Device: 1
Address Offset: 3Eh
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This register provides extensions to the PCICMD1 register that are specific to PCI-PCI bridges. The BCTRL provides additional control for the secondary interface (i.e. PCI Express Graphics) as well as some bits that affect the overall behavior of the "virtual" Host-PCI Express bridge embedded within GMCH, e.g. VGA compatible address ranges mapping.

Bit	Access & Default	Description
15:12	RO 0 h	**Reserved**
11	RO 0 b	**Discard Timer SERR Enable** Not Applicable or Implemented. Hardwired to 0.
10	RO 0 b	**Discard Timer Status** Not Applicable or Implemented. Hardwired to 0.
9	RO 0 b	**Secondary Discard Timer** Not Applicable or Implemented. Hardwired to 0.
8	RO 0 b	**Primary Discard Timer** Not Applicable or Implemented. Hardwired to 0.
7	RO 0 b	**Fast Back-to-Back Enable (FB2BEN)** Not Applicable or Implemented. Hardwired to 0.
6	R/W 0 b	**Secondary Bus Reset (SRESET)** Setting this bit triggers a hot reset on the corresponding PCI Express Port. This will force the LTSSM to transition to the Hot Reset state (via Recovery) from L0, L0s, or L1 states
5	RO 0 b	**Master Abort Mode (MAMODE)** When acting as a master, unclaimed reads that experience a master abort returns all 1's and any writes that experience a master abort completes normally and the data is thrown away. Hardwired to 0.
4	R/W 0 b	**VGA 16-bit Decode** Enables the PCI-to-PCI bridge to provide 16-bit decoding of VGA I/O address precluding the decoding of alias addresses every 1 KB. This bit only has meaning if bit 3 (VGA Enable) of this register is also set to 1, enabling VGA I/O decoding and forwarding by the bridge. 0 : Execute 10-bit address decodes on VGA I/O accesses. 1 : Execute 16-bit address decodes on VGA I/O accesses.
3	R/W 0 b	**VGA Enable (VGAEN)** Controls the routing of CPU initiated transactions targeting VGA compatible I/O and memory address ranges. See the VGAEN/MDAP table in device 0, offset 97h[0].

Bit	Access & Default	Description
2	R/W 0 b	**ISA Enable (ISAEN)** Needed to exclude legacy resource decode to route ISA resources to legacy decode path. Modifies the response by the GMCH to an I/O access issued by the CPU that target ISA I/O addresses. This applies only to I/O addresses that are enabled by the IOBASE and IOLIMIT registers. 0: All addresses defined by the IOBASE and IOLIMIT for CPU I/O transactions will be mapped to PCI Express Graphics. 1: GMCH will not forward to PCI Express Graphics any I/O transactions addressing the last 768 bytes in each 1KB block even if the addresses are within the range defined by the IOBASE and IOLIMIT registers. Instead of going to PCI Express Graphics these cycles will be forwarded to DMI where they can be subtractively or positively claimed by the ISA bridge.
1	R/W 0 b	**SERR Enable (SERREN)** 0: No forwarding of error messages from secondary side to primary side that could result in an SERR. 1: ERR_COR, ERR_NONFATAL, and ERR_FATAL messages result in SERR message when individually enabled by the Root Control register.
0	RO 0 b	**Parity Error Response Enable (PEREN)** Controls whether or not the Master Data Parity Error bit in the Secondary Status register is set when the MCH receives across the link (upstream) a Read Data Completion Poisoned TLP 0: Master Data Parity Error bit in Secondary Status register **cannot** be set. 1: Master Data Parity Error bit in Secondary Status register **can** be set..

6.2.23 PM_CAPID1—Power Management Capabilities

PCI Device: 1
Address Offset: 80h
Default Value: 1902A001
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:27	RO 19 h	**PME Support** This field indicates the power states in which this device may indicate PME wake via PCI Express messaging. D0, D3hot & D3cold. This device is not required to do anything to support D3hot & D3cold, it simply must report that those states are supported. Refer to the PCI Power Management 1.1 specification for encoding explanation and other power management details.
26	RO 0 b	**D2 -** Hardwired to 0 to indicate that the D2 power management state is NOT supported.
25	RO 0 b	**D1 -** Hardwired to 0 to indicate that the D1 power management state is NOT supported.
24:22	RO 000 b	**Auxiliary Current** Hardwired to 0 to indicate that there are no 3.3Vaux auxiliary current requirements.
21	RO 0 b	**Device Specific Initialization (DSI)** Hardwired to 0 to indicate that special initialization of this device is NOT required before generic class device driver is to use it.
20	RO 0 b	**Auxiliary Power Source (APS)** Hardwired to 0.
19	RO 0 b	**PME Clock** Hardwired to 0 to indicate this device does NOT support PME# generation.
18:16	RO 010 b	**PCI PM CAP Version** Hardwired to 02h to indicate there are 4 bytes of power management registers implemented and that this device complies with revision 1.1 of the *PCI Power Management Interface Specification*.
15:8	RO 90h / A0h	**Pointer to Next Capability** This contains a pointer to the next item in the capabilities list. This contains a pointer to the next item in the capabilities list. If MSICH (CAPL[0] @ 7Fh) is 0, then the next item in the capabilities list is the Message Signaled Interrupts (MSI) capability at 90h. If MSICH (CAPL[0] @ 7Fh) is 1, then the next item in the capabilities list is the PCI Express capability at A0h.
7:0	RO 01 h	**Capability ID** Value of 01h identifies this linked list item (capability structure) as being for PCI Power Management registers.

6.2.24 PM_CS1—Power Management Control/Status

PCI Device: 1
Address Offset: 84h
Default Value: 00000000h
Access: RO, R/W/S
Size: 32 bits

Bit	Access & Default	Description
31:16	RO 0000 h	**Reserved -**
15	RO 0 b	**PME Status** Indicates that this device does not support PME# generation from D3-cold.
14:13	RO 00 b	**Data Scale** Indicates that this device does not support the power management data register.
12:9	RO 0 h	**Data Select** Indicates that this device does not support the power management data register.
8	R/W/S 0 b	**PME Enable** Indicates that this device does not generate PME# assertion from any D-state. 0: PME# generation not possible from any D State 1: PME# generation enabled from any D State The setting of this bit has no effect on hardware. See PM_CAP[15:11]
7:2		**Reserved**
1:0	R/W 00 b	**Power State** Indicates the current power state of this device and can be used to set the device into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. 00: D0 01: D1 (Not supported in this device.) 10: D2 (Not supported in this device.) 11: D3 Support of $D3_{cold}$ does not require any special action. While in the $D3_{hot}$ state, this device can only act as the target of PCI configuration transactions (for power management control). This device also cannot generate interrupts or respond to MMR cycles in the D3 state. The device must return to the D0 state in order to be fully-functional. There is no hardware functionality required to support these Power States.

6.2.25 SS_CAPID—Subsystem ID and Vendor ID Capabilities

PCI Device: 1
Address Offset: 88h
Default Value: 0000800Dh
Access: RO
Size: 32 bits

This capability is used to uniquely identify the subsystem where the PCI device resides. Because this device is an integrated part of the system and not an add-in device, it is anticipated that this capability will never be used. However, it is necessary because Microsoft will test for its presence.

Bit	Access & Default	Description
31:16		**Reserved**
15:8	RO 80h	**Pointer to Next Capability** This contains a pointer to the next item in the capabilities list which is the PCI Power Management capability.
7:0	RO 0D h	**Capability ID** Value of 0Dh identifies this linked list item (capability structure) as being for SSID/SSVID registers in a PCI-to-PCI Bridge.

6.2.26 SS—Subsystem ID and Subsystem Vendor ID

PCI Device: 1
Address Offset: 8Ch
Default Value: 00008086h
Access: R/WO
Size: 32 bits

System BIOS can be used as the mechanism for loading the SSID/SVID values. These values must be preserved through power management transitions and a hardware reset.

Bit	Access & Default	Description
31:16	R/WO 0000 h	**Subsystem ID (SSID)** Identifies the particular subsystem and is assigned by the vendor.
15:0	R/WO 8086 h	**Subsystem Vendor ID (SSVID)** Identifies the manufacturer of the subsystem and is the same as the vendor ID which is assigned by the PCI Special Interest Group.

6.2.27 MSI_CAPID—Message Signaled Interrupts Capability ID

PCI Device: 1
Address Offset: 90h
Default Value: A005h
Access: RO
Size: 16 bits

When a device supports MSI it can generate an interrupt request to the processor by writing a predefined data item (a message) to a predefined memory address.

In that case walking this linked list will skip this capability and instead go directly from the PCI PM capability to the PCI Express capability.

Bit	Access & Default	Description
15:8	RO A0 h	**Pointer to Next Capability** This contains a pointer to the next item in the capabilities list which is the PCI Express capability.
7:0	RO 05 h	**Capability ID** 05h = identifies this linked list item (capability structure) as being for MSI registers.

6.2.28 MC—Message Control

PCI Device: 1
Address Offset: 92h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

System software can modify bits in this register, but the device is prohibited from doing so.

If the device writes the same message multiple times, only one of those messages is guaranteed to be serviced. If all of them must be serviced, the device must not generate the same message again until the driver services the earlier one.

Bit	Access & Default	Description
15:8		**Reserved**
7	RO 0 b	**64-bit Address Capable** Hardwired to 0 to indicate that the function does not implement the upper 32 bits of the Message Address register and is incapable of generating a 64-bit memory address.
6:4	R/W 000 b	**Multiple Message Enable (MME)** System software programs this field to indicate the actual number of messages allocated to this device. This number will be equal to or less than the number actually requested. 000: 1 Messages allocated 001 - 111: Reserved
3:1	RO 000 b	**Multiple Message Capable (MMC)** System software reads this field to determine the number of messages being requested by this device. 000: 1 Messages Requested 001 - 111: Reserved
0	R/W 0 b	**MSI Enable (MSIEN)** Controls the ability of this device to generate MSI's. 0: MSI will not be generated. 1: MSI will be generated when we receive PME or HotPlug messages. INTA will not be generated and INTA Status (PCISTS1[3]) will not be set.

6.2.29 MA—Message Address

PCI Device: 1
Address Offset: 94h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

A read from this register produces undefined results.

Bit	Access & Default	Description
31:2	R/W 00000000 h	**Message Address** Used by system software to assign an MSI address to the device. The device handles an MSI by writing the padded contents of the MD register to this address.
1:0	RO 00 b	**Force DWORD Align** Hardwired to 0 so that addresses assigned by system software are always aligned on a DWORD address boundary.

6.2.30 MD—Message Data

PCI Device: 1
Address Offset: 98h
Default Value: 0000h
Access: R/W
Size: 16 bits

Bit	Access & Default	Description
15:0	R/W 0000 h	**Message Data** Base message data pattern assigned by system software and used to handle an MSI from the device. When the device must generate an interrupt request, it writes a 32-bit value to the memory address specified in the MA register. The upper 16 bits are always set to 0. The lower 16 bits are supplied by this register.

6.2.31 PEG_CAPL—PCI Express Based Graphics Capability List

PCI Device: 1
Address Offset: A0h
Default Value: 0010h
Access: RO
Size: 16 bits

Enumerates the PCI Express capability structure.

Bit	Access & Default	Description
15:8	RO 00 h	**Pointer to Next Capability** This value terminates the capabilities list. The Virtual Channel capability and any other PCI Express specific capabilities that are reported via this mechanism are in a separate capabilities list located entirely within PCI Express Extended Configuration Space.
7:0	RO 10 h	**Capability ID** Identifies this linked list item (capability structure) as being for PCI Express registers.

6.2.32 PEG_CAP—PCI Express*Based Graphics Capabilities

PCI Device: 1
Address Offset: A2h
Default Value: 0141h
Access: RO
Size: 16 bits

Indicates PCI Express device capabilities.

Bit	Access & Default	Description
15:14		**Reserved**
13:9	RO 00000 b	**Interrupt Message Number** Hardwired to 0.
8	R/WO 1 b	**Slot Implemented** 0: The PCI Express Link associated with this port is connected to an integrated component or is disabled. 1: The PCI Express Link associated with this port is connected to a slot. BIOS must initialize this field appropriately if a slot connection is not implemented.
7:4	RO 4 h	**Device/Port Type** Hardwired to 0100 to indicate root port of PCI Express Root Complex.
3:0	RO 1 h	**PCI Express Capability Version** Hardwired to 1 as it is the first version.

6.2.33 DCAP—Device Capabilities

PCI Device: 1
Address Offset: A4h
Default Value: 00000000h
Access: RO
Size: 32 bits

This register indicates PCI Express link capabilities.

Bit	Access & Default	Description
31:6		**Reserved** Hardwired to 0.
5	RO 0 b	**Extended Tag Field Supported** Hardwired to indicate support for 5-bit Tags as a Requestor.
4:3	RO 00 b	**Phantom Functions Supported.** Hardwired to 0.
2:0	RO 000 b	**Max Payload Size** Hardwired to indicate 128B max supported payload for Transaction Layer Packets (TLP).

6.2.34 DCTL—Device Control

PCI Device: 1
Address Offset: A8h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Provides control for PCI Express device specific capabilities.

The error reporting enable bits are in reference to errors detected by this device, not errors messages received across the link. The reporting of error messages (ERR_CORR, ERR_NONFATAL, ERR_FATAL) received by Root Port is controlled exclusively by Root Port Command Register.

Bit	Access & Default	Description
15:8		**Reserved**
7:5	R/W 000 b	**Max Payload Size** 000: 128B max supported payload for Transaction Layer Packets (TLP). As a receiver, the Device must handle TLPs as large as the set value; as transmitter, the Device must not generate TLPs exceeding the set value. Note: All other encodings are reserved.
4		**Reserved**
3	R/W 0 b	**Unsupported Request Reporting Enable** 0 = Disabled. 1 = Enabled. Unsupported Requests will be reported. Note that reporting of error messages received by Root Port is controlled exclusively by Root Control register.
2	R/W 0 b	**Fatal Error Reporting Enable** 0 = Disabled 1 = Enabled. Fatal errors will be reported. For a Root Port, the reporting of fatal errors is internal to the root. No external ERR_FATAL message is generated.
1	R/W 0 b	**Non-Fatal Error Reporting Enable** 0 = Disabled. 1 = Enabled. Non-fatal errors will be reported. For a Root Port, the reporting of non-fatal errors is internal to the root. No external ERR_NONFATAL message is generated. Uncorrectable errors can result in degraded performance.
0	R/W 0 b	**Correctable Error Reporting Enable** 0 = Disabled. 1 = Enabled. Correctable errors will be reported. For a Root Port, the reporting of correctable errors is internal to the root. No external ERR_CORR message is generated.

6.2.35 DSTS—Device Status

PCI Device: 1
Address Offset: AAh
Default Value: 0000h
Access: RO, R/WC
Size: 16 bits

Reflects status corresponding to controls in the Device Control register.

The error reporting bits are in reference to errors detected by this device, not errors messages received across the link.

Bit	Access & Default	Description
15:6		**Reserved**
5	RO 0 b	**Transactions Pending** 0: All pending transactions (including completions for any outstanding non-posted requests on any used virtual channel) have been completed. 1: Indicates that the device has transaction(s) pending (including completions for any outstanding non-posted requests for all used Traffic Classes).
4		**Reserved**
3	R/WC 0 b	**Unsupported Request Detected** When set this bit indicates that the Device received an Unsupported Request. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control Register.
2	R/WC 0 b	**Fatal Error Detected** When set this bit indicates that fatal error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.
1	R/WC 0 b	**Non-Fatal Error Detected** When set this bit indicates that non-fatal error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register.
0	R/WC 0 b	**Correctable Error Detected** When set this bit indicates that correctable error(s) were detected. Errors are logged in this register regardless of whether error reporting is enabled or not in the Device Control register. **Note:** The GMCH may report a false 8B/10B Receiver Error when exiting L0s. This is reported thru the Correctable Error Detected bit CESTS device 1, offset 1D0h, Bit [0]. This will reduce the value of Receiver Error detection when L0s is enabled. Disable L0s for accurate Receiver Error reporting.

6.2.36 LCAP—Link Capabilities

PCI Device: 1
Address Offset: ACh
Default Value: 02012801h
Access: RO, R/WO
Size: 32 bits

Indicate PCI Express device specific capabilities.

Bit	Access & Default	Description
31:24	RO 02 h	**Port Number** Indicates the PCI Express port number for the given PCI Express link. Matches the value in Element Self Description [31:24].
23:18		**Reserved**
17:15	R/WO 010 b	**L1 Exit Latency** Indicates the length of time this Port requires to complete the transition from L1 to L0. The value 010 b indicates the range of 2 µs to less than 4 µs. If this field is required to be any value other than the default, BIOS must initialize it accordingly. Both bytes of this register that contain a portion of this field must be written simultaneously in order to prevent an intermediate (and undesired) value from ever existing.
14:12	R/WO 010 b	**L0s Exit Latency** Indicates the length of time this Port requires to complete the transition from L0s to L0. The value 010 b indicates the range of 128 ns to less than 256 ns. ***Note:*** *The default value for this field assumes a Common Clock Configuration. If the link is not in Common Clock, then System BIOS will need to program 100b (652 ns, which falls into the "512 ns to less than 1 us" range) in this field.*
11:10	W/RO 11 b	**Active State Link PM Support** L0s & L1 entry supported.
9:4	RO 010000 b	**Max Link Width** Hardwired to indicate X16. When X1 mode is enabled on this PCI Express x16 Graphics interface device, this field reflects X1 (01h).
3:0	RO 1 h	**Max Link Speed** Hardwired to indicate 2.5 Gb/s.

6.2.37 LCTL—Link Control

PCI Device: 1
Address Offset: B0h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Allows control of PCI Express link.

Bit	Access & Default	Description
15:8		**Reserved**
7	R/W 0 h	**Extended Synch** 0: Standard Fast Training Sequence (FTS). 1: Reserved
6	R/W 0 b	**Common Clock Configuration** 0: Indicates that this component and the component at the opposite end of this Link are operating with asynchronous reference clock. 1: Indicates that this component and the component at the opposite end of this Link are operating with a distributed common reference clock. Components utilize this common clock configuration information to report the correct L0s and L1 Exit Latencies.
5	R/W 0 b	**Retrain Link** 0: Normal operation 1: Full Link retraining is initiated by directing the Physical Layer LTSSM from L0, L0s, or L1 states to the Recovery state. This bit always returns 0 when read. This bit is cleared automatically (no need to write a 0).
4	R/W 0 b	**Link Disable** 0: Normal operation 1: Link is disabled Link retraining happens automatically on 1 to 0 transition, just like when coming out of reset. Writes to this bit are immediately reflected in the value read from the bit, regardless of actual Link state.
3	RO 0 b	**Read Completion Boundary (RCB)** Hardwired to 0 to indicate 64 byte.
2	RO 0 b	**Reserved**
1:0	R/W 00 b	**Active State PM** Controls the level of active state power management supported on the given link. 00: Disabled 01: L0s Entry Supported 10: L1 Entry Supported (Only) 11: L0s and L1 Entry Supported

6.2.38 LSTS—Link Status

PCI Device: 1
Address Offset: B2h
Default Value: 1001h
Access: RO
Size: 16 bits

Indicates PCI Express link status.

Bit	Access & Default	Description
15:13		**Reserved**
12	RO 1 b	**Slot Clock Configuration** 0: The device uses an independent clock irrespective of the presence of a reference on the connector. 1: The device uses the same physical reference clock that the platform provides on the connector.
11	RO 0 b	**Link Training** Indicates that the Physical Layer LTSSM is in the Configuration or Recovery state, or that 1b was written to the Retrain Link bit but Link training has not yet begun. Hardware clears this bit when the LTSSM exits the Configuration/Recovery state once Link training is complete.
10	RO 0 b	**Training Error** This bit is set by hardware upon detection of unsuccessful training of the Link to the L0 Link state.
9:4	RO 000000 b	**Negotiated Width** Indicates negotiated link width. This field is valid only when the link is in the L0, L0s, or L1 states (after link width negotiation is successfully completed). 00h: Reserved 01h: X1 04h: Reserved 08h: Reserved 10h: X16 All other encodings are reserved.
3:0	RO 1 h	**Negotiated Speed** Indicates negotiated link speed. 1h: 2.5 Gb/s All other encodings are reserved.

6.2.39 SLOTCAP—Slot Capabilities

PCI Device: 1
Address Offset: B4h
Default Value: 00000000h
Access: RO, R/WO
Size: 32 bits

PCI Express Slot related registers allow for the support of Hot Plug.

Bit	Access & Default	Description
31:19	R/WO 0000 h	**Physical Slot Number** Indicates the physical slot number attached to this Port. This field must be initialized by BIOS to a value that assigns a slot number that is globally unique within the chassis.
18:17		**Reserved**
16:15	R/WO 00 b	**Slot Power Limit Scale** Specifies the scale used for the Slot Power Limit Value. 00 = 1.0x 01 = 0.1x 10 = 0.01x 11 = 0.001x If this field is written, the link sends a Set_Slot_Power_Limit message.
14:7	R/WO 00 h	**Slot Power Limit Value** In combination with the Slot Power Limit Scale value, specifies the upper limit on power supplied by slot. Power limit (in Watts) is calculated by multiplying the value in this field by the value in the Slot Power Limit Scale field. If this field is written, the link sends a Set_Slot_Power_Limit message.
6	R/WO 0 b	**Hot-plug Capable** Indicates that this slot is capable of supporting Hot-plug operations.
5	R/WO 0 b	**Hot-plug Surprise** Indicates that a device present in this slot might be removed from the system without any prior notification.
4	R/WO 0 b	**Power Indicator Present** Indicates that a Power Indicator is implemented on the chassis for this slot.
3	R/WO 0 b	**Attention Indicator Present** Indicates that an Attention Indicator is implemented on the chassis for this slot.
2:1		**Reserved**
0	R/WO 0 b	**Attention Button Present** Indicates that an Attention Button is implemented on the chassis for this slot. The Attention Button allows the user to request hot-plug operations.

6.2.40 SLOTCTL—Slot Control

PCI Device: 1
Address Offset: B8h
Default Value: 01C0
Access: RO, R/W
Size: 16 bits

PCI Express Slot related registers allow for the support of Hot Plug.

Bit	Access & Default	Description
15:10		**Reserved**
9:8	R/W 01 b	**Power Indicator Control** Reads to this register return the current state of the Power Indicator. Writes to this register set the Power Indicator and cause the Port to send the appropriate POWER_INDICATOR_* messages. 00: Reserved 01: On 10: Blink 11: Off
7:6	R/W 11 b	**Attention Indicator Control** Reads to this register return the current state of the Attention Indicator. Writes to this register set the Attention Indicator and cause the Port to send the appropriate ATTENTION_INDICATOR_* messages. 00: Reserved 01: On 10: Blink 11: Off
5	R/W 0 b	**Hot plug Interrupt Enable** When set enables generation of hot plug interrupt on enabled hot plug events.
4	R/W 0 b	**Command Completed Interrupt Enable** When set enables the generation of hot plug interrupt when a command is completed by the Hot plug controller.
3	R/W 0 b	**Presence Detect Changed Enable** When set enables the generation of hot plug interrupt or wake message on a presence detect changed event.
2:1		**Reserved**
0	R/W 0 b	**Attention Button Pressed Enable** When set enables the generation of hot plug interrupt or wake message on an attention button pressed event.

6.2.41 SLOTSTS—Slot Status

PCI Device: 1
Address Offset: BAh
Default Value: 0000h
Access: RO, R/WC
Size: 16 bits

PCI Express Slot related registers allow for the support of Hot Plug.

Bit	Access & Default	Description
15:7	RO 000 h	**Reserved**
6	RO X b	**Presence Detect State** Indicates the presence of a card in the slot. 0 : Slot Empty 1 : Card Present in slot.
5		Reserved
4	R/WC 0 b	**Command Completed** Set when the hot plug controller completes an issued command.
3	R/WC 0 b	**Presence Detect Changed** Set when a Presence Detect change is detected. This corresponds to an edge on the signal that corresponds to bit 6 of this register (Presence Detect State).
2:1		Reserved
0	R/WC 0 b	**Attention Button Pressed** Set when the Attention Button is pressed.

6.2.42 RCTL—Root Control

PCI Device: 1
Address Offset: BCh
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Allows control of PCI Express Root Complex specific parameters. The system error control bits in this register determine if corresponding SERRs are generated when our device detects an error (reported in this device's Device Status register) or when an error message is received across the link. Reporting of SERR as controlled by these bits takes precedence over the SERR Enable in the PCI Command Register.

Bit	Access & Default	Description
15:4		**Reserved**
3	R/W 0 b	**PME Interrupt Enable** 0: No interrupts are generated as a result of receiving PME messages. 1: Enables interrupt generation upon receipt of a PME message as reflected in the PME Status bit of the Root Status Register. A PME interrupt is also generated if the PME Status bit of the Root Status Register is set when this bit is set from a cleared state.
2	R/W 0 b	**System Error on Fatal Error Enable** Controls the Root Complex's response to fatal errors. 0: No SERR generated on receipt of fatal error. 1: Indicates that an SERR should be generated if a fatal error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.
1	R/W 0 b	**System Error on Non-Fatal Uncorrectable Error Enable** Controls the Root Complex's response to non-fatal errors. 0: No SERR generated on receipt of non-fatal error. 1: Indicates that an SERR should be generated if a non-fatal error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.
0	R/W 0 b	**System Error on Correctable Error Enable** Controls the Root Complex's response to correctable errors. 0: No SERR generated on receipt of correctable error. 1: Indicates that an SERR should be generated if a correctable error is reported by any of the devices in the hierarchy associated with this Root Port, or by the Root Port itself.

6.2.43 RSTS—Root Status

PCI Device: 1
Address Offset: C0h
Default Value: 00000000h
Access: RO, R/W/C
Size: 32 bits

Provides information about PCI Express Root Complex specific parameters.

Bit	Access & Default	Description
31:18		**Reserved**
17	RO 0 b	**PME Pending** Indicates that another PME is pending when the PME Status bit is set. When the PME Status bit is cleared by software; the PME is delivered by hardware by setting the PME Status bit again and updating the Requestor ID appropriately. The PME pending bit is cleared by hardware if no more PME's are pending.
16	R/W/C 0 b	**PME Status** Indicates that PME was asserted by the requestor ID indicated in the PME Requestor ID field. Subsequent PME's are kept pending until the status register is cleared by writing a 1 to this field.
15:0	RO 0000 h	**PME Requestor ID** Indicates the PCI requestor ID of the last PME requestor.

6.2.44 PEGLC—PCI Express* Based Graphics Legacy Control

PCI Device: 1
Address Offset: ECh
Default Value 00000000h
Access: RO, R/W
Size: 32 bits

Controls functionality that is needed by Legacy (non-PCI Express aware) OS's during run time.

Bit	Access & Default	Description
31:3	RO 0000 0000h	**Reserved**
2	R/W 0 b	**PME GPE Enable** (PMEGPE) 0: Do not generate GPE PME message when PME is received. 1: Generate a GPE PME message when PME is received (Assert_PMEGPE and Deassert_PMEGPE messages on DMI). This enables the MCH to support PMEs on the PEG port under legacy OSs.
1	R/W 0 b	**Hot-Plug GPE Enable** (HPGPE) 0: Do not generate GPE Hot-Plug message when Hot-Plug event is received. 1: Generate a GPE Hot-Plug message when Hot-Plug Event is received (Assert_HPGPE and Deassert_HPGPE messages on DMI). This enables the MCH to support Hot-Plug on the PEG port under legacy OSs.
0	R/W 0 b	**General Message GPE Enable (GENGPE)** 0: Do not forward received GPE assert/deassert messages. 1: Forward received GPE assert/deassert messages. These general GPE message can be received via the PEG port from an external Intel device (i.e. PxH) and will be subsequently forwarded to the ICH (via Assert_GPE and Deassert_GPE messages on DMI). For example, a PxH might send this message if a PCI Express device is hot plugged into a PxH downstream port.

6.2.45 VCECH—Virtual Channel Enhanced Capability Header

PCI Device: 1
Address Offset: 100h
Default Value: 14010002h
Access: RO
Size: 32 bits

Indicates PCI Express device Virtual Channel capabilities.

Note that extended capability structures for PCI Express devices are located in PCI Express extended configuration space and have different field definitions than standard PCI capability structures.

Bit	Access & Default	Description
31:20	RO 140 h	**Pointer to Next Capability** The Link Declaration Capability is the next in the PCI Express extended capabilities list.
19:16	RO 1 h	**PCI Express Virtual Channel Capability Version** Hardwired to 1 to indicate compliances with the 1.0 version of the PCI Express specification.
15:0	RO 0002 h	**Extended Capability ID** Value of 0002 h identifies this linked list item (capability structure) as being for PCI Express Virtual Channel registers.

6.2.46 PVCCAP1—Port VC Capability Register 1

PCI Device: 1
Address Offset: 104h
Default Value: 00000001h
Access: RO, R/WO
Size: 32 bits

Describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access & Default	Description
31:7		**Reserved**
6:4	RO 000 b	**Low Priority Extended VC Count** Indicates the number of (extended) Virtual Channels in addition to the default VC belonging to the low-priority VC (LPVC) group that has the lowest priority with respect to other VC resources in a strict-priority VC Arbitration. The value of 0 in this field implies strict VC arbitration.
3		**Reserved**
2:0	R/WO 001 b	**Extended VC Count** Indicates the number of (extended) Virtual Channels in addition to the default VC supported by the device.

6.2.47 PVCCAP2—Port VC Capability Register 2

PCI Device: 1
Address Offset: 108h
Default Value: 00000000h
Access: RO
Size: 32 bits

Describes the configuration of PCI Express Virtual Channels associated with this port.

Bit	Access & Default	Description
31:24	RO 00 h	**VC Arbitration Table Offset** Indicates the location of the VC Arbitration Table. This field contains the zero-based offset of the table in DQWORDS (16 bytes) from the base address of the Virtual Channel Capability Structure. A value of 0 indicates that the table is not present (due to fixed VC priority).
23:8		**Reserved**
7:0	RO 01 h	**VC Arbitration Capability** Indicates that the only possible VC arbitration scheme is hardware fixed (in the root complex). VC1 is the highest priority, VC0 is the lowest priority.

6.2.48 PVCCTL—Port VC Control

PCI Device: 1
Address Offset: 10Ch
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15:4		**Reserved**
3:1	R/W 000 b	**VC Arbitration Select** This field will be programmed by software to the only possible value as indicated in the VC Arbitration Capability field. This field can not be modified when more than one VC in the LPVC group is enabled.
0		**Reserved**

6.2.49 VC0RCAP—VC0 Resource Capability

PCI Device: 1
Address Offset: 110h
Default Value: 00000000h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:16		**Reserved**
15	RO 0 b	**Reject Snoop Transactions** 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1: Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:0		**Reserved**

6.2.50 VC0RCTL—VC0 Resource Control

PCI Device: 1
Address Offset: 114h
Default Value: 800000FF
Access: RO, R/W
Size: 32 bits

Controls the resources associated with PCI Express Virtual Channel 0.

Bit	Access & Default	Description
31	RO 1 b	**VC0 Enable** For VC0 this is hardwired to 1 and read only as VC0 can never be disabled.
30:27		**Reserved**
26:24	RO 000 b	**VC0 ID** Assigns a VC ID to the VC resource. For VC0 this is hardwired to 0 and read only.
23:8		**Reserved**
7:1	R/W 1111111 b	**TC/VC0 Map** Indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO 1 b	**TC0/VC0 Map** Traffic Class 0 is always routed to VC0.

6.2.51 VC0RSTS—VC0 Resource Status

PCI Device: 1
Address Offset: 11Ah
Default Value: 0000h
Access: RO
Size: 16 bits

Reports the Virtual Channel specific status.

Bit	Access & Default	Description
15:2		**Reserved**
1	RO 1 b	**VC0 Negotiation Pending** 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling). This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0		**Reserved**

6.2.52 VC1RCAP—VC1 Resource Capability

PCI Device: 1
Address Offset: 11Ch
Default Value: 00008000h
Access: RO
Size: 32 bits

Bit	Access & Default	Description
31:16		**Reserved**
15	RO 1 b	**Reject Snoop Transactions** 0: Transactions with or without the No Snoop bit set within the TLP header are allowed on this VC. 1: Any transaction without the No Snoop bit set within the TLP header will be rejected as an Unsupported Request.
14:0		**Reserved**

6.2.53 VC1RCTL—VC1 Resource Control

PCI Device: 1
Address Offset: 120h
Default Value: 01000000h
Access: RO, R/W
Size: 32 bits

Controls the resources associated with PCI Express Virtual Channel 1.

Bit	Access & Default	Description
31	R/W 0 b	**VC1 Enable** 0: Virtual Channel is disabled. 1: Virtual Channel is enabled. See exceptions in note below. Software must use the VC Negotiation Pending bit to check whether the VC negotiation is complete. When VC Negotiation Pending bit is cleared, a 1 read from this VC Enable bit indicates that the VC is enabled (Flow Control Initialization is completed for the PCI Express port); a 0 read from this bit indicates that the Virtual Channel is currently disabled. **NOTES**: 1. To enable a Virtual Channel, the VC Enable bits for that Virtual Channel must be set in both Components on a Link. 2. To disable a Virtual Channel, the VC Enable bits for that Virtual Channel must be cleared in both Components on a Link. 3. Software must ensure that no traffic is using a Virtual Channel at the time it is disabled. 4. Software must fully disable a Virtual Channel in both Components on a Link before re-enabling the Virtual Channel.
30:27		**Reserved**
26:24	R/W 001 b	**VC1 ID** Assigns a VC ID to the VC resource. Assigned value must be non-zero. This field can not be modified when the VC is already enabled.
23:8		**Reserved**
7:1	R/W 0000000 b	**TC/VC1 Map** Indicates the TCs (Traffic Classes) that are mapped to the VC resource. Bit locations within this field correspond to TC values. For example, when bit 7 is set in this field, TC7 is mapped to this VC resource. When more than one bit in this field is set, it indicates that multiple TCs are mapped to the VC resource. In order to remove one or more TCs from the TC/VC Map of an enabled VC, software must ensure that no new or outstanding transactions with the TC labels are targeted at the given Link.
0	RO 0 b	**TC0/VC1 Map** Traffic Class 0 is always routed to VC0.

6.2.54 VC1RSTS—VC1 Resource Status

PCI Device: 1
Address Offset: 126h
Default Value: 0000h
Access: RO
Size: 16 bits

Reports the Virtual Channel specific status.

Bit	Access & Default	Description
15:2		**Reserved**
1	RO 1 b	**VC1 Negotiation Pending** 0: The VC negotiation is complete. 1: The VC resource is still in the process of negotiation (initialization or disabling). Software may use this bit when enabling or disabling the VC. This bit indicates the status of the process of Flow Control initialization. It is set by default on Reset, as well as whenever the corresponding Virtual Channel is Disabled or the Link is in the DL_Down state. It is cleared when the link successfully exits the FC_INIT2 state Before using a Virtual Channel, software must check whether the VC Negotiation Pending fields for that Virtual Channel are cleared in both Components on a Link.
0		**Reserved**

6.2.55 RCLDECH—Root Complex Link Declaration Enhanced Capability Header

PCI Device: 1
Address Offset: 140h
Default Value: 00010005h
Access: RO
Size: 32 bits

This capability declares links from this element (PEG) to other elements of the root complex component to which it belongs. See PCI Express specification for link/topology declaration requirements.

Bit	Access & Default	Description
31:20	RO 000 h	**Pointer to Next Capability** This is the last capability in the PCI Express extended capabilities
19:16	RO 1 h	**Link Declaration Capability Version** Hardwired to 1 to indicate compliances with the 1.0 version of the PCI Express specification.
15:0	RO 0005 h	**Extended Capability ID** Value of 0005 h identifies this linked list item (capability structure) as being for PCI Express Link Declaration Capability.

6.2.56 ESD—Element Self Description

PCI Device: 1
Address Offset: 144h
Default Value: 02000100h
Access: RO, R/WO
Size: 32 bits

Provides information about the root complex element containing this Link Declaration Capability.

Bit	Access & Default	Description
31:24	RO 02 h	**Port Number** Specifies the port number associated with this element with respect to the component that contains this element. This port number value is utilized by the egress port of the component to provide arbitration to this Root Complex Element.
23:16	R/WO 00 h	**Component ID** Identifies the physical component that contains this Root Complex Element. Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. The value only needs to be written in one of the mirrored fields and it will be reflected everywhere that it is mirrored.
15:8	RO 01 h	**Number of Link Entries** Indicates the number of link entries following the Element Self Description. This field reports 1 (to Egress port only as we don't report any peer-to-peer capabilities in our topology).
7:4		**Reserved**
3:0	RO 0 h	**Element Type** Indicates the type of the Root Complex Element. Value of 0 h represents a root port.

6.2.57 LE1D—Link Entry 1 Description

PCI Device: 1
Address Offset: 150h
Default Value: 00000000h
Access: RO, R/WO
Size: 32 bits

First part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
31:24	RO 00 h	**Target Port Number** Specifies the port number associated with the element targeted by this link entry (Egress Port). The target port number is with respect to the component that contains this element as specified by the target component ID.
23:16	R/WO 00 h	**Target Component ID** Identifies the physical or logical component that is targeted by this link entry. A value of 0 is reserved; Component IDs start at 1. This value is a mirror of the value in the Component ID field of all elements in this component. The value only needs to be written in one of the mirrored fields and it will be reflected everywhere that it is mirrored.
15:2		**Reserved**
1	RO 0 b	**Link Type** Indicates that the link points to memory-mapped space (for RCRB). The link address specifies the 64-bit base address of the target RCRB.
0	R/WO 0 b	**Link Valid** 0: Link Entry is not valid and will be ignored. 1: Link Entry specifies a valid link.

6.2.58 LE1A—Link Entry 1 Address

PCI Device: 1
Address Offset: 158h
Default Value: 0000000000000000h
Access: RO, R/WO
Size: 64 bits

Second part of a Link Entry which declares an internal link to another Root Complex Element.

Bit	Access & Default	Description
63:32		**Reserved**
31:12	R/WO 0 0000 h	**Link Address** Memory mapped base address of the RCRB that is the target element (Egress Port) for this link entry.
11:0		**Reserved**

6.2.59 PEGSSTS—PCI Express Graphics Sequence Status

PCI Device: 1
Address Offset: 218h
Default Value: 0000000000000FFFh
Access: RO
Size: 64 bits

PCI Express status reporting that is required by the PCI Express spec.

Bit	Access & Default	Description
63:60		**Reserved**
59:48	RO 000 h	**Next Retry Buffer Entry Sequence Number** This is the sequence number to be applied to and pre-pended to the next TLP being placed into the Retry Buffer at the Transaction Layer/Data Link Layer interface.
47:44		**Reserved**
43:32	RO 000 h	**Next Transmitted Sequence Number** This is the sequence number to be applied to and pre-pended to the next outgoing TLP. This value is taken from the outlet of the Retry Buffer (the current sequence number being transmitted on the PCI Express Link).
31:28		**Reserved**
27:16	RO 000 h	**Next Receive Sequence Number** This is the sequence number associated with the TLP that is expected to be received next.
15:12		**Reserved**
11:0	RO FFF h	**Last Acknowledged Sequence Number** This is the sequence number associated with the last acknowledged TLP.

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7 Internal Graphics Device #2 Configuration Register (D2:F0)

Note: Excludes Mobile Intel® 915PM Express Chipset.

Device #2 contains registers for the internal graphics functions. The table below lists the PCI configuration registers in order of ascending offset address.

Function #0 can be VGA compatible or not, this is selected through bit 1 of GGC register (Device #0, offset 52h)

The following sections describe Device 2 PCI configuration registers only.

Note: Register information for the PCI Express* Based Graphics Port is NOT relative to the Intel® 915GMS , 910GML and 910GMLE Express Chipsets.

Note: Register information for the Integrated Graphics Device is NOT relative to the Mobile Intel® 915PM Express Chipset.



7.1 Device #2: Function 0 Register Summary

7.2 Device #2: Function 0 Configuration Register Details

Table 7-1. Device #2: Function 0 Configuration Register Summary Table

Address Start (h)	Register Symbol	Register Name	Default Value	Access
00-01h	VID2	Vendor Identification	8086h	RO
02-03h	DID2	Device Identification	2592h	RO
04-05h	PCICMD2	PCI Command	00h	RO, R/W
06-07h	PCISTS2	PCI Status	0090h	RO, R/WC
08h	RID2	Revision Identification	00h	RO
09-0Bh	CC	Class Code	030000h	RO
0Ch	CLS	Cache Line Size	00h	RO
0Dh	MLT2	Master Latency Timer	00h	RO
0Eh	HDR2	Header Type	80h	RO
0Fh		***Reserved***		
10-13h	MMADR	Memory Mapped Range Address	00000000h	RO, R/W
14-17h	IOBAR	I/O Base Address	00000001h	RO, R/W
18-1Bh	GMADR	Graphics Memory Range Address	00000000h	RO, R/W, R/W/L
1C-1Fh	GTTADR	Graphics Translation Table Range Address	00000000h	RO, R/W
20-2Bh		***Reserved***		
2C-2Dh	SVID2	Subsystem Vendor Identification	0000h	R/WO
2E-2Fh	SID2	Subsystem Identification	0000h	R/WO
30-33h	ROMADR	Video BIOS ROM Base Address	00000000h	RO
34h	CAPPOINT	Capabilities Pointer	D0h	RO
35-3Bh		***Reserved***		
3Ch	INTRLINE	Interrupt Line	00h	R/W
3Dh	INTRPIN	Interrupt Pin	01h	RO
3Eh	MINGNT	Minimum Grant	00h	RO
3Fh	MAXLAT	Maximum Latency	00h	RO
40-43h		***Reserved***		
44h	MCAPPTR	Mirror of Dev0 Capability Pointer		
45-47h		***Reserved***		

Address Start (h)	Register Symbol	Register Name	Default Value	Access
48-50h	MCAPID	Mirror of Dev0 Capability Identification		
51h		***Reserved***		
52-53h	MGGC	Mirror of Dev0 GMCH Graphics Control		
54-57h	MDEVENdev0f0	Mirror of Dev0 Device Enable		
58-5Bh		***Reserved***		
5C-5Fh	BSM	Base of Stolen Memory	07800000h	RO
60-61h		***Reserved***		
62h	MSAC	Multi Size Aperture Control	00h	RO, R/W
63-CFh		***Reserved***		
D0-D1h	PMCAPID	Power Management Capabilities ID	0001h	RO
D2-D3h	PMCAP	Power Management Capabilities	0022h	RO
D4-D5h	PMCS	Power Management Control/Status	0000h	RO, R/W
D6-DFh		***Reserved***		
E0-E1h	SWSMI	Software SMI	0000h	R/W
E2-E3h		***Reserved***		
E4-E7	ASLE	System Display Event	00000000h	R/W
E9-EFh		***Reserved***		
F0-F1h	GCFGC	Graphics Clock Frequency and Gating Control	0000h	RO, R/W
F2-F3h	GCPLLC	Graphics Clock PLL Control	3464h	RO, R/W
F4-FBh	ASLE	ASL Event /Legacy Backlight Brightness	00000000h	R/W
FC-FFh	ASLS	ASL Storage	00000000h	R/W

7.2.1 VID2—Vendor Identification

PCI Device: 2
Function: 0
Address Offset: 00h
Default Value: 8086h
Access: RO
Size: 16 bits

This register combined with the Device Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 8086 h	**Vendor Identification Number (VID):** PCI standard identification for Intel.

7.2.2 DID2—Device Identification

PCI Device: 2
Function: 0
Address Offset: 02h
Default Value: 2592h
Access: RO
Size: 16 bits

This register combined with the Vendor Identification register uniquely identifies any PCI device.

Bit	Access & Default	Description
15:0	RO 2592 h	**Device Identification Number (DID):** Identifier assigned to the GMCH core/primary PCI device.

7.2.3 PCICMD2—PCI Command

PCI Device: 2
Function: 0
Address Offset: 04h
Default Value: 00h
Access: RO, R/W
Size: 16 bits

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI compliant master accesses to main memory.

Bit	Access & Default	Description
15:11		**Reserved.**
10	R/W 0 b	**Interrupt Disable:** This bit disables the device from asserting INTx#. 0: Enable the assertion of this device's INTx# signal. 1: Disable the assertion of this device's INTx# signal. DO_INTx messages will not be sent to DMI.
9	RO 0 b	**Fast Back-to-Back (FB2B)**: Not Implemented. Hardwired to 0.
8	RO 0 b	**SERR Enable (SERRE):** Not Implemented. Hardwired to 0.
7	RO 0 b	**Address/Data Stepping Enable (ADSTEP):** Not Implemented. Hardwired to 0.
6	RO 0 b	**Parity Error Enable (PERRE):** Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.
5	RO 0 b	**Video Palette Snooping (VPS):** This bit is hardwired to 0 to disable snooping.
4	RO 0 b	**Memory Write and Invalidate Enable (MWIE):** Hardwired to 0. The IGD does not support memory write and invalidate commands.
3	RO 0 b	**Special Cycle Enable (SCE):** This bit is hardwired to 0. The IGD ignores Special cycles.
2	R/W 0 b	**Bus Master Enable (BME):** 0: Disable IGD bus mastering. 1: Enable the IGD to function as a PCI compliant master.
1	R/W 0 b	**Memory Access Enable (MAE)**: This bit controls the IGD's response to memory space accesses. 0: Disable. 1: Enable.
0	R/W 0 b	**I/O Access Enable (IOAE):** This bit controls the IGD's response to I/O space accesses. 0: Disable. 1: Enable.

7.2.4 PCISTS2—PCI Status

PCI Device: 2
Function: 0
Address Offset: 06h
Default Value: 0090h
Access: RO, R/WC
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant master abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

Bit	Access & Default	Description
15	RO 0 b	**Detected Parity Error (DPE):** Since the IGD does not detect parity, this bit is always hardwired to 0.
14	RO 0 b	**Signaled System Error (SSE):** The IGD never asserts SERR#, therefore this bit is hardwired to 0.
13	RO 0 b	**Received Master Abort Status (RMAS):** The IGD never gets a Master Abort, therefore this bit is hardwired to 0.
12	RO 0 b	**Received Target Abort Status (RTAS):** The IGD never gets a Target Abort, therefore this bit is hardwired to 0.
11	RO 0 b	**Signaled Target Abort Status (STAS):** Hardwired to 0. The IGD does not use target abort semantics.
10:9	RO 00 b	**DEVSEL Timing (DEVT):** N/A. These bits are hardwired to 00.
8	RO 0 b	**Master Data Parity Error Detected (DPD):** Since Parity Error Response is hardwired to disabled (and the IGD does not do any parity detection), this bit is hardwired to 0**.**
7	RO 1 b	**Fast Back-to-Back (FB2B):** Hardwired to 1. The IGD accepts fast back-to-back when the transactions are not to the same agent.
6	RO 0 b	**User Defined Format (UDF).** Hardwired to 0.
5	RO 0 b	**66 MHz PCI Capable (66C).** N/A - Hardwired to 0.
4	RO 1 b	**Capability List (CLIST):** This bit is set to 1 to indicate that the register at 34h provides an offset into the function's PCI Configuration Space containing a pointer to the location of the first item in the list.
3	R/WC 0 b	**Interrupt Status:** This bit reflects the state of the interrupt in the device. Only when the Interrupt Disable bit in the command register is a 0 and this Interrupt Status bit is a 1, will the devices INTx# signal be asserted. Setting the Interrupt Disable bit to a 1 has no effect on the state of this bit.
2:0		**Reserved**

7.2.5 RID2—Revision Identification

PCI Device: 2
Function: 0
Address Offset: 08h
Default Value: 00h
Access: RO
Size: 8 bits

This register contains the revision number for Device #2 Functions 0 and 1

Bit	Access & Default	Description
7:0	RO 00 h	**Revision Identification Number (RID):** This is an 8-bit value that indicates the revision identification number for the GMCH.

7.2.6 CC—Class Code

PCI Device: 2
Function: 0
Address Offset: 09h
Default Value: 030000h
Access: RO
Size: 24 bits

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Bit	Access & Default	Description
23:16	RO 03 h	**Base Class Code (BCC)** This is an 8-bit value that indicates the base class code for the GMCH. This code has the value 03h, indicating a Display Controller.
15:8	RO 00 h	**Sub-Class Code (SUBCC):** Based on Device #0 DAFC[VGA Disable], which is also mirrored in device #2 MDAFCdev0f0[VGA Disable] 00h: VGA compatible 80h: Non VGA
7:0	RO 00 h	**Programming Interface (PI)** 00h: Hardwired as a Display controller.

7.2.7 CLS—Cache Line Size

PCI Device: 2
Function: 0
Address Offset: 0Ch
Default Value: 00h
Access: RO
Size: 8 bits

The IGD does not support this register as a PCI slave.

Bit	Access & Default	Description
7:0	RO 00 h	**Cache Line Size (CLS)** This field is hardwired to 0s. The IGD as a PCI compliant master does not use the Memory Write and Invalidate command and, in general, does not perform operations based on cache line size.

7.2.8 MLT2—Master Latency Timer

PCI Device: 2
Function: 0
Address Offset: 0Dh
Default Value: 00h
Access: RO
Size: 8 bits

The IGD does not support the programmability of the master latency timer because it does not perform bursts.

Bit	Access & Default	Description
7:0	RO 00 h	**Master Latency Timer Count Value** Hardwired to 0s.

7.2.9 HDR2—Header Type

PCI Device: 2
Function: 0
Address Offset: 0Eh
Default Value: 80h
Access: RO
Size: 8 bits

This register contains the Header Type of the IGD.

Bit	Access & Default	Description
7	RO 1 b	**Multi Function Status (MFunc)** Indicates if the device is a Multi-Function Device. The Value of this register is determined by Device #0, offset 54h, DEVEN[4].. If Device #0 DEVEN[4] is set, the MFunc bit is also set.
6:0	RO 0000000 b	**Header Code (H)** This is an 7-bit value that indicates the Header Code for the IGD. This code has the value 00h, indicating a type 0 configuration space format.

7.2.10 MMADR—Memory Mapped Range Address

PCI Device: 2
Function: 0
Address Offset: 10h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

This register requests allocation for the IGD registers and instruction ports. The allocation is for 512 kB and the base address is defined by bits [31:19].

Bit	Access & Default	Description
31:19	R/W 0000 h	**Memory Base Address:** Set by the OS, these bits correspond to address signals [31:19].
18:4	RO 0000 h	**Address Mask:** Hardwired to 0s to indicate 512 KB address range.
3	RO 0 b	**Prefetchable Memory:** Hardwired to 0 to prevent pre-fetching.
2:1	RO 00 b	**Memory Type:** Hardwired to 0s to indicate 32-bit address.
0	RO 0 b	**Memory / IO Space:** Hardwired to 0 to indicate memory space.

7.2.11 IOBAR—I/O Base Address

PCI Device: 2
Function: 0
Address Offset: 14h
Default Value: 00000001h
Access: RO, R/W
Size: 32 bits

This register provides the Base offset of the I/O registers within Device #2. Bits 15:3 are programmable allowing the I/O Base to be located anywhere in 16bit I/O Address Space. Bits 2:1 are fixed and return zero, bit 0 is hardwired to a one indicating that 8 bytes of I/O space are decoded.

Access to the 8Bs of IO space is allowed in PM state D0 when IO Enable (PCICMD bit 0) set. Access is disallowed in PM states D1-D3 or if IO Enable is clear or if Device #2 is turned off or if Internal graphics is disabled. Note that access to this IO BAR is independent of VGA functionality within Device #2. Also note that this mechanism in available only through function 0 of Device#2 and is not duplicated in function #1.

If accesses to this IO bar are allowed then the GMCH claims all 8, 16 or 32 bit IO cycles from the CPU that falls within the 8B claimed.

Bit	Access & Default	Description
31:16		**Reserved.**
15:3	R/W 0000 h	**IO Base Address:** Set by the OS, these bits correspond to address signals [15:3].
2:1	RO 00 b	**Memory Type:** Hardwired to 0s to indicate 32-bit address.
0	RO 1 b	**Memory / IO Space:** Hardwired to **1** to indicate **I/O** space.

7.2.12 GMADR—Graphics Memory Range Address

PCI Device: 2
Function: 0
Address Offset: 18h
Default Value: 00000000h
Access: RO, R/W, R/W/L
Size: 32 bits

IGD graphics memory base address is specified in this register.

Bit	Access & Default	Description
31:28	R/W 0 h	**Memory Base Address:** Set by the OS, these bits correspond to address signals [31:28].
27	R/W/L 0 b	**256 MB Address Mask:** This bit is either part of the Memory Base Address (R/W) or part of the Address Mask (RO), depending on the value of MSAC[1]. See MSAC (Dev 2, Func 0, offset 62) for details.
26:4	RO 000000 h	**Address Mask:** Hardwired to 0s to indicate at least 128 B address range
3	RO 1 b	**Prefetchable Memory:** Hardwired to 1 to enable prefetching
2:1	RO 00 b	**Memory Type:** Hardwired to 0 to indicate 32-bit address.
0	RO 0 b	**Memory/IO Space:** Hardwired to 0 to indicate memory space.

7.2.13 GTTADR—Graphics Translation Table Range Address

PCI Device: 2
Function: 0
Address Offset: 1Ch
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

This register requests allocation for Graphics Translation Table Range. The allocation is for 256 kB and the base address is defined by bits [31:18].

Bit	Access & Default	Description
31:18	R/W 0000 h	**Memory Base Address:** Set by the OS, these bits correspond to address signals [31:18].
17:4	RO 0000 h	**Address Mask:** Hardwired to 0s to indicate 256 kB address range.
3	RO 0 b	**Prefetchable Memory:** Hardwired to 0 to prevent prefetching.
2:1	RO 00 b	**Memory Type:** Hardwired to 0s to indicate 32-bit address.
0	RO 0 b	**Memory/IO Space:** Hardwired to 0 to indicate memory space.

7.2.14 SVID2—Subsystem Vendor Identification

PCI Device: 2
Function: 0
Address Offset: 2Ch
Default Value: 0000h
Access: R/WO
Size: 16 bits

Bit	Access & Default	Description
15:0	R/WO 0000 h	**Subsystem Vendor ID.** This value is used to identify the vendor of the subsystem. This register should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This register can only be cleared by a Reset.

7.2.15 SID2—Subsystem Identification

PCI Device: 2
Function: 0
Address Offset: 2Eh
Default Value: 0000h
Access: R/WO
Size: 16 bits

Bit	Access & Default	Description
15:0	R/WO 0000 h	**Subsystem Identification.** This value is used to identify a particular subsystem. This field should be programmed by BIOS during boot-up. Once written, this register becomes Read Only. This register can only be cleared by a Reset.

7.2.16 ROMADR—Video BIOS ROM Base Address

PCI Device: 2
Function: 0
Address Offset: 30h
Default Value: 00000000h
Access: RO
Size: 32 bits

The IGD does not use a separate BIOS ROM, therefore this register is hardwired to 0s.

Bit	Access & Default	Description
31:18	RO 0000 h	**ROM Base Address:** Hardwired to 0's.
17:11	RO 00 h	**Address Mask:** Hardwired to 0s to indicate 256 KB address range.
10:1		**Reserved.**
0	RO 0 b	**ROM BIOS Enable:** 0 = ROM not accessible.

7.2.17 CAPPOINT—Capabilities Pointer

PCI Device: 2
Function: 0
Address Offset: 34h
Default Value: D0h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO D0 h	**Capabilities Pointer Value.** This field contains an offset into the function's PCI Configuration Space for the first item in the New Capabilities Linked List, the Power Management Capabilities ID registers at address D0h.

7.2.18 INTRLINE—Interrupt Line

PCI Device: 2
Function: 0
Address Offset: 3Ch
Default Value: 00h
Access: R/W
Size: 8 bits

Bit	Access & Default	Description
7:0	R/W 00 h	**Interrupt Connection.** Used to communicate interrupt line routing information. POST software writes the routing information into this register as it initializes and configures the system. The value in this register indicates which input of the system interrupt controller that the device's interrupt pin is connected to.

7.2.19 INTRPIN—Interrupt Pin

PCI Device: 2
Function: 0
Address Offset: 3Dh
Default Value: 01h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 01 h	**Interrupt Pin.** As a single function device, the IGD specifies INTA# as its interrupt pin. 01h: INTA#.

7.2.20 MINGNT—Minimum Grant

PCI Device: 2
Function: 0
Address Offset: 3Eh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00 h	**Minimum Grant Value.** The IGD does not burst as a PCI compliant master.

7.2.21 MAXLAT—Maximum Latency

PCI Device: 2
Function: 0
Address Offset: 3Fh
Default Value: 00h
Access: RO
Size: 8 bits

Bit	Access & Default	Description
7:0	RO 00 h	**Maximum Latency Value.** The IGD has no specific requirements for how often it needs to access the PCI bus.

7.2.22 MCAPPTR—Mirror of Dev0 Capability Pointer (Mirrored_D0_34)

PCI Device: 2
Function: 0
Address Offset: 44h
Size: 8 bits

This register is a Read-Only copy of Device 0, Offset 34h register.

7.2.23 MCAPID—Mirror of Dev0 Capability Identification (Mirrored_D0_E0)

PCI Device: 2
Function: 0
Address Offset: 48h
Size: 72 bits

This register is a Read-Only copy of Device 0, Offset E0h register.

7.2.24 MGGC—Mirror of Dev0 GMCH Graphics Control (Mirrored_D0_52)

PCI Device: 2
Function: 0
Address Offset: 52h
Size: 16 bits

This register is a Read-Only copy of Device 0, Offset 52h register.

7.2.25 MDEVENdev0f0—Mirror of Dev0 Device Enable (Mirrored_D0_54)

PCI Device: 2
Function: 0
Address Offset: 54h
Size: 32 bits

This register is a Read-Only copy of Device 0, Offset 54h register.

7.2.26 BSM—Base of Stolen Memory

PCI Device: 2
Function: 0
Address Offset: 5Ch
Default Value: 07800000h
Access: RO
Size: 32 bits

Graphics Stolen Memory and TSEG are within DRAM space defined under TOLUD. From the top of low used DRAM, GMCH claims 1 to 64MBs of DRAM for internal graphics if enabled.

Bit	Access & Default	Description
31:20	RO 078 h	**Base of Stolen Memory (BSM):** This register contains bits 31 to 20 of the base address of stolen DRAM memory. The host interface determines the base of Graphics Stolen memory by subtracting the graphics stolen memory size from TOLUD. See Device 0 TOLUD for more explanation.
19:0		**Reserved**

7.2.27 MSAC—Multi Size Aperture Control

PCI Device: 2
Function: 0
Address Offset: 62h
Default Address: 00h
Access: RO, R/W
Size: 8 bits

This register determines the size of the graphics memory aperture in function 0 and in the trusted space. By default, the aperture size is 256 MB (bit 27 read only). If bit 1 is set to a 1, then the aperture size is limited to 128 MB. Only the system BIOS will write this register based on pre-boot address allocation efforts, but the graphics may read this register to determine the correct aperture size. System BIOS needs to save this value on boot so that it can reset it correctly during S3 resume.

Bit	Access & Default	Description
7:4	R/W 0 h	**Scratch Bits Only --** Have no physical effect on hardware
3:2		**Reserved**
1	R/W 0 b	**256MB Aperture Disable** 0: Bit 27 of GMADR and the equivalent trusted memory aperture is read-only, allowing 256 MB of address space to be mapped. 1: Bit 27 of GMADR and the equivalent trusted memory aperture is read-write, limiting the address space to 128 MB.
0		**Reserved**

7.2.28 GDRST—Graphics Debug Reset (D2:F0)

PCI Device: 2
Address Offset: C0h
Default Value: 00h
Access: RO, R/W
Size: 8 bits

Bit	Access & Default	Description
7:2		**Reserved**
1	RO 0 b	**Graphics Reset Status** 0: Graphics subsystem not in Reset. 1: Graphics Subsystem in Reset as a result of Graphics Debug Reset. This bit gets is set to a '1' when Graphics debug reset bit is set to a '1' and the Graphics hardware has completed the debug reset sequence and all Graphics assets are in reset. This bit is cleared when Graphics Debug Reset bit is set to a '0'.
0	R/W 0 b	**Graphics Debug Reset:** 1 = assert display and render domain reset 0 = de-assert display and render domain reset Render and Display clock domain resets should be asserted for at least 20 µsecs. Once this bit is set to a "1" all GFX core MMIO registers are returned to power on default state. Device 2 IO registers are not available. Device 2 Config registers are available when Graphics debug reset is asserted.

7.2.29 PMCAPID—Power Management Capabilities ID

PCI Device: 2
Function: 0
Address Offset: D0h
Default Value: 0001h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:8	RO 00 h	**NEXT_PTR.** This contains a pointer to next item in capabilities list. This is the final capability in the list and must be set to 00h.
7:0	RO 01 h	**CAP_ID.** SIG defines this ID is 01h for power management.

7.2.30 PMCAP—Power Management Capabilities

PCI Device: 2
Function: 0
Address Offset: D2h
Default Value: 0022h
Access: RO
Size: 16 bits

Bit	Access & Default	Description
15:11	RO 00000 b	**PME Support.** This field indicates the power states in which the IGD may assert PME#. Hardwired to 0 to indicate that the IGD does not assert the PME# signal.
10	RO 0 b	**D2.** The D2 power management state is not supported. This bit is hardwired to 0.
9	RO 0 b	**D1.** Hardwired to 0 to indicate that the D1 power management state is not supported.
8:6		**Reserved**
5	RO 1 b	**Device Specific Initialization (DSI).** Hardwired to 1 to indicate that special initialization of the IGD is required before generic class device driver is to use it.
4	RO 0 b	**Auxiliary Power Source.** Hardwired to 0.
3	RO 0 b	**PME Clock.** Hardwired to 0 to indicate IGD does not support PME# generation.
2:0	RO 010 b	**Version.** Hardwired to 010b to indicate that there are 4 bytes of power management registers implemented and that this device complies with revision 1.1 of the PCI Power Management Interface Specification

7.2.31 PMCS—Power Management Control/Status

PCI Device: 2
Function: 0
Address Offset: D4h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15	RO 0 b	**PME_Status:** This bit is 0 to indicate that IGD does not support PME# generation from D3 (cold).
14:9		**Reserved**
8	RO 0 b	**PME_En:** This bit is 0 to indicate that PME# assertion from D3 (cold) is disabled.
7:2		**Reserved**
1:0	R/W 00 b	**PowerState:** This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. On a transition from D3 to D0 the graphics controller is optionally reset to initial values. Behavior of the graphics controller in supported states is detailed in the power management section. **Bits[1:0] Power state** 00 D0 **Default** 01 D1 **Not Supported** 10 D2 **Not Supported** 11 D3

7.2.32 SWSMI—Software SMI

PCI Device: 2
Function: 0
Address Offset: E0h
Default Value: 0000h
Access: R/W
Size: 16 bits

As long as there is the potential that DVO port legacy drivers exist which expect this register at this address, Dev#2F0address E0h-E1h must be reserved for this register.

Bit	Access & Default	Description
15:8	R/W 00 h	**SW scratch bits**
7:1	R/W 00 h	**Software Flag** Used to indicate caller and SMI function desired, as well as return result
0	R/W 0 b	**GMCH Software SMI Event** When Set this bit will trigger an SMI. Software must write a 0 to clear this bit

7.2.33 GCFGC—Graphics Clock Frequency and Gating Control

PCI Device: 2
Function: 0
Address Offset: F0h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15:14	R/W 0 b	**Reserved**
13	R/W 0 b	**GFX GVL low frequency Enable.** 0 = Do not Use GFX GVL low frequency target for Render Clock. 1 = Use GFX GVL low frequency target for Render Clock.
12	R/W 0 b	**GFX GVL low frequency target**. 0 = 133 MHz (Default Value). 1 = Reserved.
11	R/W 0 b	**Gate Core Render Clock (GCRC):** 0: Core render clock (crclk) is running 1: Core render clock (crclk) is gated
10	R/W 0 b	**Asynchronously Change Core Render Clock (ACCRC):** A 0 to 1 transition on this bit will immediately load new pre- and post-divider values for the crclk and crx2clk. Writing 1 to 1, 1 to 0, and 0 to 0 have no effect.
9	R/W 0 b	**Gate Core Display Clock (GCRC):** 0: Core display clock (cdclk) is running 1: Core display clock (cdclk) is gated
8	R/W 0 b	**Asynchronously Change Core Display Clock (ACCDC):** A 0 to 1 transition on this bit will immediately load new pre- and post-divider values for the cdclk. Writing 1 to 1, 1 to 0, and 0 to 0 have no effect.
7	R/W 0 b	**Core Display Low Frequency Enable** 0 = Do not Use low frequency target (133 MHz) for Display Clock. 1 = Use low frequency target (133 MHz) for Display Clock. NOTE: If using 133 MHz cdclk,, Please refer to the PRD for max display resolution
6:4	R/W 000 b	**Graphics Core Display Clock Select.** 000 = 190/200 MHz (Intel 915GM / 915GME / 915GMS & Intel 910GML / 910GMLE) 001 - 011 = Reserved 100 = 333 MHz (Intel 915GM / 915GME @ 1.5 V only) 101 - 111 = Reserved
3		Reserved
2:0	R/W 000 b	**Graphics Core Render Clock Select.** 000 = 160/166 MHz (Intel 915GM / 915GME / 915GMS & Intel 910GML / 910GMLE) 001 = 190/200 MHz (Intel 915GM) 010 – 011 = Reserved 100 = 333 MHz (Intel 915GM / 915GME @ 1.5 V only) 101 - 111 = Reserved

7.2.34 LBB—Legacy Backlight Brightness

PCI Device: 2
Function: 0
Address Offset: F4h
Size: 32 bits

This register can be accessed by either Byte, Word, or Dword PCI config cycles. A write to this register will cause the Backlight Event (Display B Interrupt) if enabled.

Bit	Description
31:24	LBPC Scratch Trigger 3 – When written, this scratch byte triggers an interrupt when LBEE is enabled in the Pipe B Status register and the Display B Event is enabled in IER and unmasked in IMR etc. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
23-16	LBPC Scratch Trigger 2 – When written, this scratch byte triggers an interrupt when LBEE is enabled in the Pipe B Status register and the Display B Event is enabled in IER and unmasked in IMR etc. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
15-8	LBPC Scratch Trigger 1 – When written, this scratch byte triggers an interrupt when LBEE is enabled in the Pipe B Status register and the Display B Event is enabled in IER and unmasked in IMR etc. If written as part of a 16-bit or 32-bit write, only one interrupt is generated in common.
7:0	Legacy Backlight Brightness The value of zero is the lowest brightness setting and 255 is the brightest.

7.2.35 ASLS—ASL Storage

PCI Device: 2
Function: 0
Address Offset: FCh
Default Value: 00000000h
Access: R/W
Size: 32 bits

This software scratch register only needs to be read/write accessible. The exact bit register usage must be worked out in common between System BIOS and driver software, but storage for switching/indicating up to 6 devices is possible with this amount. For each device, the ASL control method with require two bits for _DOD (BIOS detectable yes or no, VGA/NonVGA), one bit for _DGS (enable/disable requested), and two bits for _DCS (enabled now/disabled now, connected or not).

Bit	Access & Default	Description
31:0	R/W 00000000 h	RW according to a software controlled usage to support device switching

7.2.36 Device #2 Function 1 Configuration Register Details

Table 7-2. Device #2 Function 1 Configuration Register Summary Table

Address offset (h)	Register Symbol	Register Name	Default Value	Access
00-01h	VID2	Vendor Identification		
02-03h	DID2	Device Identification		
04-05h	PCICMD2	PCI Command	0000h	RO, R/W
06-07h	PCISTS2	PCI Status	0090h	RO
08h	RID2	Revision Identification		
09-0Bh	CC	Class Code Register	038000h	RO
0Ch	CLS	Cache Line Size		
0Dh	MLT2	Master Latency Timer		
0Eh	HDR2	Header Type Register		
0Fh		***Reserved (1 B)***		
10-13h	MMADR	Memory Mapped Range Address	00000000h	RO, R/W
14-2Bh		***Reserved (24 B)***		
2C-2Dh	SVID2	Subsystem Vendor Identification		
2E-2Fh	SID2	Subsystem Identification		
30-33h	ROMADR	Video BIOS ROM Base Address		
34h	CAPPOINT	Capabilities Pointer		
35-3Dh		***Reserved (9 B)***		
3Eh	MINGNT	Minimum Grant Register		
3Fh	MAXLAT	Maximum Latency		
40-43h		***Reserved (4 B)***		
44h	MCAPPTR	Mirror of Dev0 Capability Pointer		
45-47h		***Reserved***		
48-50h	MCAPID	Mirror of Dev0 Capability Identification		
51h		***Reserved***		
52-53h	MGGC	Mirror of Dev0 GMCH Graphics Control		
54-57h	MDEVENdev 0f0	Mirror of Dev0 Device Enable		
58-5Bh		***Reserved***		
5C-5Fh	BSM	Base of Stolen Memory Register		
60-C0h		***Reserved***		
C1-C2h		***Reserved***		
C3-CFh		***Reserved***		

Address offset (h)	Register Symbol	Register Name	Default Value	Access
D0-D1h	PMCAPID	Power Management Capabilities ID		
D2-D3h	PMCAP	Power Management Capabilities		
D4-D5h	PMCS	Power Management Control/Status	0000h	RO, R/W
D6-DFh		***Reserved***		
E0-E1h	SWSMI	Software SMI		
E2-F3h		***Reserved***		
F4-F7h	LBB	Legacy Backlight Brightness		
FC-FFh	ASLS	ASL Storage	00000000h	R/W

7.2.37 VID2—Vendor Identification

PCI Device: 2
Function: 1
Address Offset: 00h
Size: 16 bits

This register is a Read Only copy of Function 0. Write attributes as D2:F0. It is implemented as common hardware with two access addresses.

7.2.38 DID2—Device Identification

PCI Device: 2
Function: 1
Address Offset: 02h
Size: 16 bits

This register is unique in Function 1 (the Function 0 DID is separate). This difference in Device ID is necessary for allowing distinct Plug and Play enumeration of function 1 when both function 0 and function 1 have the same class code.

Bit	Access & Default	Description
15:0	RO 2790h	**Device Identification Number (DID):** This is a 16 bit value assigned to the GMCH Graphic device Function 1

7.2.39 PCICMD2—PCI Command

PCI Device: 2
Function: 1
Address Offset: 04h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

This 16-bit register provides basic control over the IGD's ability to respond to PCI cycles. The PCICMD Register in the IGD disables the IGD PCI compliant master accesses to main memory.

Bit	Access & Default	Description
15:10		**Reserved.**
9	RO 0 b	**Fast Back-to-Back (FB2B)**: Not Implemented. Hardwired to 0.
8	RO 0 b	**SERR Enable (SERRE):** Not Implemented. Hardwired to 0.
7	RO 0 b	**Address/Data Stepping Enable (ADSTEP):** Not Implemented. Hardwired to 0.
6	RO 0 b	**Parity Error Enable (PERRE):** Not Implemented. Hardwired to 0. Since the IGD belongs to the category of devices that does not corrupt programs or data in system memory or hard drives, the IGD ignores any parity error that it detects and continues with normal operation.
5	RO 0 b	**VGA Palette Snoop Enable (VGASNOOP):** This bit is hardwired to 0 to disable snooping.
4	RO 0 b	**Memory Write and Invalidate Enable (MWIE):** Hardwired to 0. The IGD does not support memory write and invalidate commands.
3	RO 0 b	**Special Cycle Enable (SCE):** This bit is hardwired to 0. The IGD ignores Special cycles.
2	R/W 0 b	**Bus Master Enable (BME):** Set to 1 to enable the IGD to function as a PCI compliant master. Set to 0 to disable IGD bus mastering.
1	R/W 0 b	**Memory Access Enable (MAE):** This bit controls the IGD's response to memory space accesses. 0: Disable. 1: Enable.
0	R/W 0 b	**I/O Access Enable (IOAE):** This bit controls the IGD's response to I/O space accesses. 0: Disable. 1: Enable.

7.2.40 PCISTS2—PCI Status

PCI Device: 2
Function: 1
Address Offset: 06h
Default Value: 0090h
Access: RO
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of a PCI compliant master abort and PCI compliant target abort. PCISTS also indicates the DEVSEL# timing that has been set by the IGD.

Bit	Access & Default	Description
15	RO 0 b	**Detected Parity Error (DPE):** Since the IGD does not detect parity, this bit is always hardwired to 0.
14	RO 0 b	**Signaled System Error (SSE):** The IGD never asserts SERR#, therefore this bit is hardwired to 0.
13	RO 0 b	**Received Master Abort Status (RMAS):** The IGD never gets a Master Abort, therefore this bit is hardwired to 0.
12	RO 0 b	**Received Target Abort Status (RTAS):** The IGD never gets a Target Abort, therefore this bit is hardwired to 0.
11	RO 0 b	**Signaled Target Abort Status (STAS):** Hardwired to 0. The IGD does not use target abort semantics.
10:9	RO 00 b	**DEVSEL Timing (DEVT):** These bits are hardwired to "00".
8	RO 0 b	**Master Data Parity Error Detected (DPD):** Since Parity Error Response is hardwired to disabled (and the IGD does not do any parity detection), this bit is hardwired to 0**.**
7	RO 1 b	**Fast Back-to-Back (FB2B):** Hardwired to 1. The IGD accepts fast back-to-back when the transactions are not to the same agent.
6	RO 0 b	**User Defined Format (UDF).** Hardwired to 0.
5	RO 0 b	**66 MHz PCI Capable (66C).** N/A - Hardwired to 0.
4	RO 1 b	**Capability List (CLIST):** This bit is set to 1 to indicate that the register at 34h provides an offset into the function's PCI Configuration Space containing a pointer to the location of the first item in the list.
3	RO 0 b	**Interrupt Status:** Hardwired to 0.
2:0		**Reserved**

7.2.41 RID2—Revision Identification

PCI Device: 2
Function: 1
Address Offset: 08h
Size: 8 bits

This register is a copy of Function 0. It has the same Read, Write attributes as Function 0. It is implemented as common hardware with two access addresses.

7.2.42 CC—Class Code Register

PCI Device: 2
Function: 1
Address Offset: 09h
Default Value: 038000h
Access: RO
Size: 24 bits

This register contains the device programming interface information related to the Sub-Class Code and Base Class Code definition for the IGD. This register also contains the Base Class Code and the function sub-class in relation to the Base Class Code.

Bit	Access & Default	Description
23:16	RO 03 h	**Base Class Code (BCC)** This is an 8-bit value that indicates the base class code for the GMCH. This code has the value 03h, indicating a Display Controller.
15:8	RO 80 h	**Sub-Class Code (SUBCC)** 80h: Non VGA
7:0	RO 00 h	**Programming Interface (PI)** 00h: Hardwired as a Display controller.

7.2.43 CLS—Cache Line Size

PCI Device: 2
Function: 1
Address Offset: 0Ch
Size: 8 bits

This register is a Read Only copy of Function 0.

7.2.44 MLT2—Master Latency Timer

PCI Device: 2
Function: 1
Address Offset: 0Dh
Size: 8 bits

This register is a Read Only copy of Function 0.

7.2.45 HDR2—Header Type Register

PCI Device: 2
Function: 1
Address Offset: 0Eh
Size: 8 bits

This register is a Read Only copy of Function 0.

7.2.46 MMADR—Memory Mapped Range Address

PCI Device: 2
Function: 1
Address Offset: 10h
Default Value: 00000000h
Access: RO, R/W
Size: 32 bits

This register requests allocation for the IGD registers and instruction ports. The allocation is for 512 kB and the base address is defined by bits [31:19].

Bit	Access & Default	Description
31:19	R/W 0000 h	**Memory Base Address:** Set by the OS, these bits correspond to address signals [31:19].
18:4	RO 0000 h	**Address Mask:** Hardwired to 0s to indicate 512 kB address range.
3	RO 0 b	**Prefetchable Memory:** Hardwired to 0 to prevent prefetching.
2:1	RO 00 b	**Memory Type:** Hardwired to 0s to indicate 32-bit address.
0	RO 0 b	**Memory / IO Space:** Hardwired to 0 to indicate memory space.

7.2.47 SVID2—Subsystem Vendor Identification

PCI Device: 2
Function: 1
Address Offset: 2Ch
Size: 16 bits

This register is a Read Only copy of Function 0. It has the same Read-Write attributes as D2:F0. It is implemented as common hardware with two access addresses.

7.2.48 SID2—Subsystem Identification

PCI Device: 2
Function: 1
Address Offset: 2Eh
Size: 16 bits

This register is a Read Only copy of Function 0.

7.2.49 ROMADR—Video BIOS ROM Base Address

PCI Device: 2
Function: 1
Address Offset: 30h
Size: 32 bits

This register is a Read Only copy of Function 0. It has the same Read-Write attributes as D2:F0. It is implemented as common hardware with two access addresses.

7.2.50 CAPPOINT—Capabilities Pointer

PCI Device: 2
Function: 1
Address Offset: 34h
Size: 8 bits

This register is a Read Only copy of Function 0. It has the same Read-Write attributes as D2:F0. It is implemented as common hardware with two access addresses.

7.2.51 MINGNT—Minimum Grant Register

PCI Device: 2
Function: 1
Address Offset: 3Eh
Size: 8 bits

This register is a Read Only copy of Function 0. It has the same Read-Write attributes as D2:F0. It is implemented as common hardware with two access addresses.

7.2.52 MAXLAT—Maximum Latency

PCI Device: 2
Function: 1
Address Offset: 3Fh
Size: 8 bits

This register is a Read Only copy of Function 0. It has the same Read-Write attributes as D2:F0. It is implemented as common hardware with two access addresses.



7.2.53 MCAPPTR—Mirror of Dev0 Capability Pointer (Mirrored_D0_34)

PCI Device: 2
Function: 1
Address Offset: 44h
Size: 8 bits

This register is a Read-Only copy of Device 0, Offset 34h register.

7.2.54 MCAPID—Mirror of Dev0 Capability Identification (Mirrored_D0_E0)

PCI Device: 2
Function: 1
Address Offset: 48h
Size: 72 bits

This register is a Read-Only copy of Device 0, Offset E0h register.

7.2.55 MGGC—Mirror of Dev0 GMCH Graphics Control (Mirrored_D0_52)

PCI Device: 2
Address Offset: 52h
Size: 16 bits

This register is a Read-Only copy of Device 0, Offset 52h register.

7.2.56 MDEVENdev0f0—Mirror of Dev0 Device Enable (Mirrored_D0_54)

PCI Device: 2
Function: 1
Address Offset: 54h
Size: 32 bits

This register is a Read-Only copy of Device 0, Offset 54h register.

7.2.57 BSM—Base of Stolen Memory Register

PCI Device: 2
Function: 1
Address Offset: 5Ch
Size: 32 bits

This register is a Read Only copy of Function 0

7.2.58 PMCAPID—Power Management Capabilities ID

PCI Device: 2
Function: 1
Address Offset: D0h
Size: 16 bits

This register is a copy of Function 0. It has the same Read, Write attributes as Function 0. It is implemented as common hardware with two access addresses.

7.2.59 PMCAP—Power Management Capabilities

PCI Device: 2
Function: 1
Address Offset: D2h
Size: 16 bits

This register is a copy of Function 0. It has the same Read, Write attributes as Function 0. It is implemented as common hardware with two access addresses.

7.2.60 PMCS—Power Management Control/Status

PCI Device: 2
Function: 1
Address Offset: D4h
Default Value: 0000h
Access: RO, R/W
Size: 16 bits

Bit	Access & Default	Description
15	RO 0 b	**PME_Status:** This bit is 0 to indicate that IGD does not support PME# generation from D3 (cold).
14:9		**Reserved:** The IGD does not support data register. This bit always returns 0 when read, write operations have no effect.
8	RO 0 b	**PME_En:** This bit is 0 to indicate that PME# assertion from D3 (cold) is disabled.
7:2		**Reserved.**
1:0	R/W 00 b	**PowerState:** This field indicates the current power state of the IGD and can be used to set the IGD into a new power state. If software attempts to write an unsupported state to this field, write operation must complete normally on the bus, but the data is discarded and no state change occurs. On a transition from D3 to D0 the graphics controller is optionally reset to initial values. **Bits[1:0] Power state** 00 D0 **Default** 01 D1 **Not Supported** 10 D2 **Not Supported** 11 D3

7.2.61 SWSMI—Software SMI

PCI Device: 2
Function: 1
Address Offset: E0h
Size: 16 bits

This register is a copy of Function 0. It has the same Read, Write attributes as Function 0. It is implemented as common hardware with two access addresses.

7.2.62 LBB—Legacy Backlight Brightness

PCI Device: 2
Function: 1
Address offset: F4h
Size: 32 bits

This register is a copy of Function 0. It has the same Read, Write attributes as Function 0. It is implemented as common hardware with two access addresses.

7.2.63 ASLS—ASL Storage

PCI Device: 2
Function: 1
Address Offset: FCh
Default Value: 00000000h
Access: R/W
Size: 32 bits

This software scratch register only needs to be read/write accessible. The exact bit register usage must be worked out in common between System BIOS and driver software, but storage for switching/indicating up to 6 devices is possible with this amount. For each device, the ASL control method with require two bits for _DOD (BIOS detectable yes or no, VGA/NonVGA), one bit for _DGS (enable/disable requested), and two bits for _DCS (enabled now/disabled now, connected or not).

Bit	Access & Default	Description
31:0	R/W 00000000 h	R/W according to a software controlled usage to support device switching

7.3 Device #2 – PCI I/O Registers

The following are not PCI config registers; they are I/O registers. This mechanism allows access to internal graphics MMIO registers must not be used to access VGA IO registers which are mapped through the MMIO space. VGA registers must be accessed directly through the dedicated VGA IO ports.

7.3.1 MMIO Index—MMIO Address Register

I/O Address: IOBAR + 0h
Default Value: 00000000h
Access: R/W
Size: 32 bits

MMIO_INDEX: A 32 bit IO write to this port loads the **offset** of the MMIO register that needs to be accessed. An IO Reads returns the current value of this register. An 8/16 bit IO write to this register is completed by the GMCH but does not update this register. This mechanism allows access to internal graphics MMIO registers must not be used to access VGA IO registers which are mapped through the MMIO space. VGA registers must be accessed directly through the dedicated VGA IO ports.

Bit	Access & Default	Description
31:2	R/W 00000000 h	**Register/GTT Offset:** This field selects any one of the DWORD registers within the MMIO register space of Device #2.
1:0	R/W 00 b	**Reserved**

7.3.2 MMIO Data—MMIO Data Register

I/O Address: IOBAR + 4h
Default Value: 00000000h
Access: R/W
Size: 32 bits

MMIO_DATA A 32 bit IO write to this port is re-directed to the MMIO register location pointed to by the MMIO-index register. A 32 bit IO read to this port is re-directed to the MMIO register address pointed to by the MMIO-index register regardless of the target selection in MMIO_INDEX(1:0). 8-bit or 16-bit IO writes are completed by the GMCH and may have un-intended side effects, hence must not be used to access the data port. 8-bit or 16-bit IO reads are completed normally.

Bit	Access & Default	Description
31:0	R/W 00000000 h	**MMIO data window**

§



8 System Address Map

The GMCH supports 4 GB of addressable memory space and 64 kB+3 of addressable I/O space. There is a programmable memory address space under the 1-MB region which is divided into regions which can be individually controlled with programmable attributes such as Disable, Read/Write, Write Only, or Read Only. Attribute programming is described in the Register Description section. This section focuses on how the memory space is partitioned and what the separate memory regions are used for. I/O address space has simpler mapping and is explained near the end of this section.

Addressing of memory ranges larger than 4 GB is NOT supported. The HREQ [4:3] FSB pins are decoded to determine whether the access is above or below 4 GB.

The GMCH does not support the PCI Dual Address Cycle (DAC) Mechanism, PCI Express 64-bit prefetchable memory transactions, or any other addressing mechanism that allows addressing of greater than 4 GB on either the DMI or PCI Express interface. The GMCH does not limit DRAM space in hardware. There is no hardware lock to stop someone from inserting more memory than is addressable.

In the following sections, it is assumed that all of the compatibility memory ranges reside on the DMI. The exception to this rule is VGA ranges, which may be mapped to PCI Express, DMI, or to the internal graphics device (IGD). In the absence of more specific references, cycle descriptions referencing PCI should be interpreted as the DMI/PCI, while cycle descriptions referencing PCI Express or IGD are related to the PCI Express bus or the internal graphics device respectively. The GMCH does not remap APIC or any other memory spaces above TOLUD (Top of Low Usable DRAM). The TOLUD register is set to the appropriate value by BIOS.

The Address Map includes a number of programmable ranges:

Device 0:

EPBAR Egress port registers. Necessary for setting up VC1 as an isochronous channel. (4 kB window)

MCHBAR Memory mapped range for internal GMCH registers. For example, memory buffer register controls. (16 kB window)

PCIEXBAR Flat memory-mapped address spaced to access device configuration registers. This mechanism can be used to access PCI configuration space (0-FFh) and Extended configuration space (100h-FFFh) for PCI Express devices. This enhanced configuration access mechanism is defined in the PCI Express specification. (256-MB window).

DMIBAR This window is used to access registers associated with the MCH/ICH (DMI) register memory range. (4 kB window)

GGC – GMCH graphics control register. Used to select the amount of main memory that is pre-allocated to support the internal graphics device in VGA (non-linear) and Native (linear) modes. (0-64 MB options).

Device 1, Function 0:

MBASE1/MLIMIT1 – PCI Express port non-prefetchable memory access window.

PMBASE1/PMLIMIT1 – PCI Express port prefetchable memory access window.

IOBASE1/IOLIMIT1 – PCI Express port IO access window.

Device 2, Function 0:

MMADR – IGD registers and internal graphics instruction port. (512 kB window)

IOBAR – I/O access window for internal graphics. Through this window address/data register pair, using I/O semantics, the IGD and internal graphics instruction port registers can be accessed.

GMADR – Internal graphics translation window. (256-MB window)

GTTADR – Internal graphics translation table location. (256 kB window).

Device 2, Function 1:

MMADR – Function 1 IGD registers and internal graphics instruction port. (512 kB window)

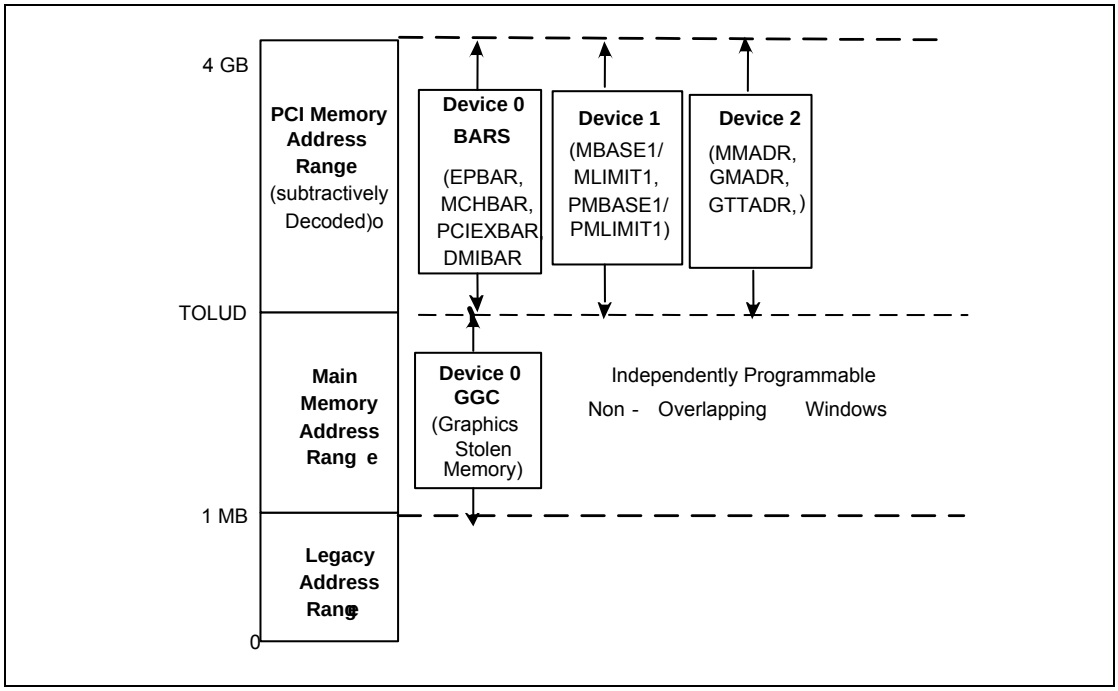
IOBAR – Function 1 IO access window for internal graphics.

The rules for the above programmable ranges are:

1. ALL of these ranges MUST be unique and NON-OVERLAPPING. It is the BIOS or system designer's responsibility to limit memory population so that adequate PCI, PCI Express, High BIOS, PCI Express Memory Mapped space, and APIC memory space can be allocated.
2. In the case of overlapping ranges with memory, the memory decode will be given priority.
3. There are NO Hardware Interlocks to prevent problems in the case of overlapping ranges.
4. Accesses to overlapped ranges may produce indeterminate results.
5. The only peer-to-peer cycles allowed below the top of memory (register TOLUD) are DMI to PCI Express VGA range writes. Note that peer to peer cycles to the Internal Graphics VGA range are not supported.

The following figure represents system memory address map in a simplified form.

Figure 8-1. System Address Ranges

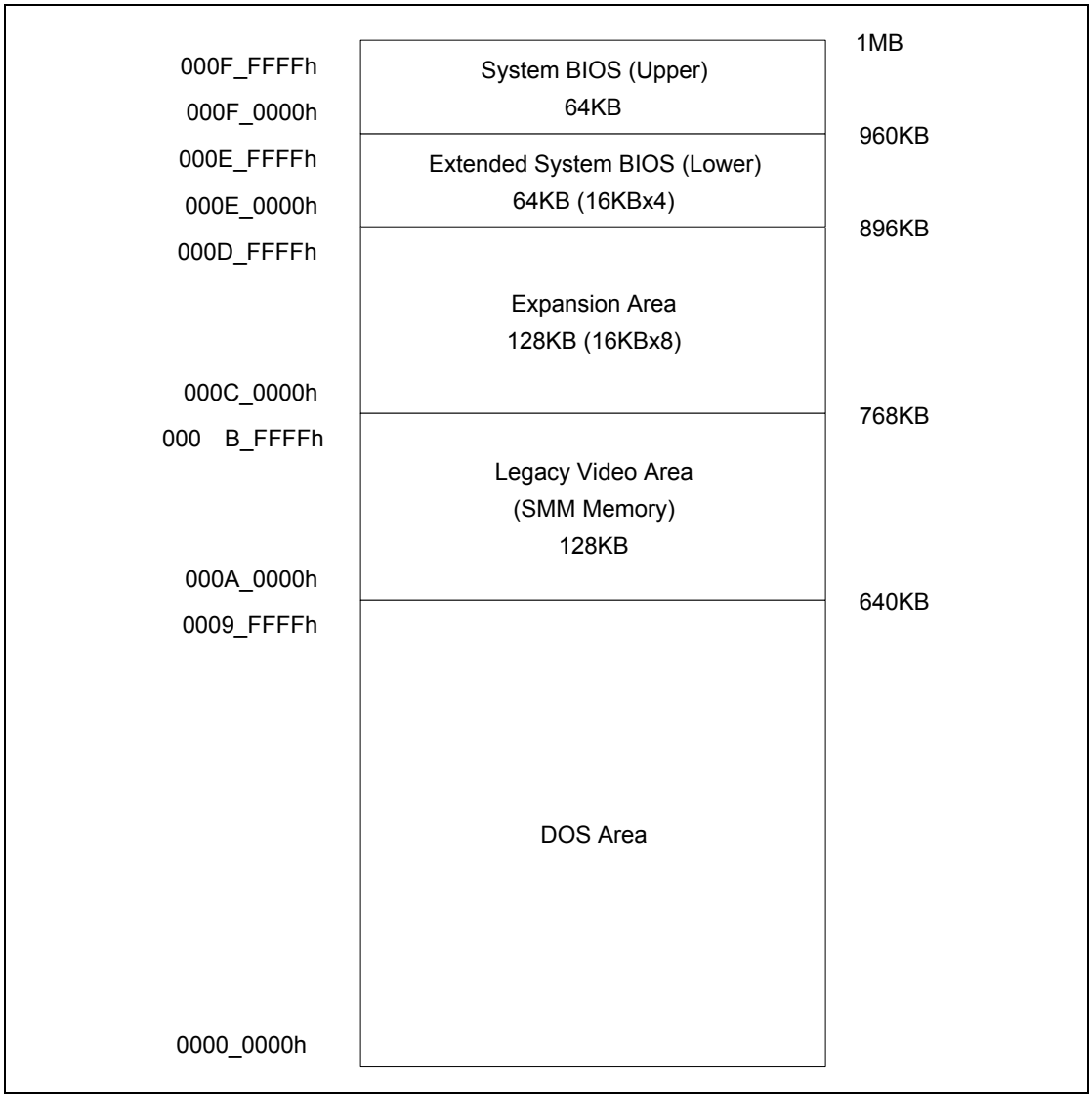


8.1 Legacy Address Range

This area is divided into the following address regions:

0 - 640 kB – DOS Area
640 - 768 kB – Legacy Video Buffer Area
768 - 896 kB in 16 kB sections (total of eight sections) – Expansion Area
896 -960 kB in 16 kB sections (total of four sections) – Extended System BIOS Area
960 kB - 1 MB memory – system BIOS Area

Figure 8-2. DOS Legacy Address Range





8.1.1 DOS Range (0h – 9_FFFFh)

The DOS area is 640 kB (0000_0000h – 0009_FFFFh) in size and is always mapped to the main memory controlled by the GMCH.

8.1.2 Legacy Video Area (A_0000h-B_FFFFh)

The legacy 128 kB VGA memory range, frame buffer, (000A_0000h – 000B_FFFFh) can be mapped to IGD (Device #2), to PCI Express (Device #1), and/or to the DMI. The appropriate mapping depends on which devices are enabled and the programming of the VGA steering bits. Based on the VGA steering bits, priority for VGA mapping is constant. The GMCH always decodes internally mapped devices first. Internal to the GMCH, decode precedence is always given to IGD. The GMCH always positively decodes internally mapped devices, namely the IGD and PCI Express. Subsequent decoding of regions mapped to PCI Express or the DMI depends on the Legacy VGA configuration bits (VGA Enable and MDAP). This region is also the default for SMM space.

Compatible SMRAM Address Range (A_0000h-B_FFFFh)

When compatible SMM space is enabled, SMM-mode CPU accesses to this range are routed to physical system DRAM at 000A 0000h - 000B FFFFh. Non-SMM-mode CPU accesses to this range are considered to be to the Video Buffer Area as described above. PCI Express and DMI originated cycles to enabled SMM space are not allowed and are considered to be to the Video Buffer Area if IGD is not enabled as the VGA device. PCI Express and DMI initiated cycles are attempted as Peer cycles, and will master abort on PCI if no external VGA device claims them.

Monochrome Adapter (MDA) Range (B_0000h-B_7FFFh)

Legacy support requires the ability to have a second graphics controller (monochrome) in the system. Accesses in the standard VGA range are forwarded to IGD, PCI Express, or the DMI (depending on configuration bits). Since the monochrome adapter may be mapped to any one of these devices, the GMCH must decode cycles in the MDA range (000B_0000h - 000B_7FFFh) and forward either to IGD, PCI Express, or the DMI. This capability is controlled by a VGA steering bits and the legacy configuration bit (MDAP bit). In addition to the memory range B0000h to B7FFFh, the GMCH decodes IO cycles at 3B4h, 3B5h, 3B8h, 3B9h, 3BAh and 3BFh and forwards them to the either IGD, PCI Express, and/or the DMI.

8.1.3 Expansion Area (C_0000h-D_FFFFh)

This 128 kB ISA Expansion region (000C_0000h – 000D_FFFFh) is divided into eight 16 KB segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, read/write, or disabled. Typically, these blocks are mapped through GMCH and are subtractively decoded to ISA space. Memory that is disabled is not remapped.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

Table 8-1. Expansion Area Memory Segments

Memory Segments	Attributes	Comments
0C0000H - 0C3FFFH	W/R	Add-on BIOS
0C4000H - 0C7FFFH	W/R	Add-on BIOS
0C8000H - 0CBFFFH	W/R	Add-on BIOS
0CC000H - 0CFFFFH	W/R	Add-on BIOS
0D0000H - 0D3FFFH	W/R	Add-on BIOS
0D4000H - 0D7FFFH	W/R	Add-on BIOS
0D8000H - 0DBFFFH	W/R	Add-on BIOS
0DC000H - 0DFFFFH	W/R	Add-on BIOS

8.1.4 Extended System BIOS Area (E_0000h-E_FFFFh)

This 64 kB area (000E_0000h – 000E_FFFFh) is divided into four, 16 kB segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main DRAM or to DMI. Typically, this area is used for RAM or ROM. Memory segments that are disabled are not remapped elsewhere.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

Table 8-2. Extended System BIOS Area Memory Segments

Memory Segments	Attributes	Comments
0E0000H - 0E3FFFH	W/R	BIOS Extension
0E4000H - 0E7FFFH	W/R	BIOS Extension
0E8000H - 0EBFFFH	W/R	BIOS Extension
0EC000H - 0EFFFFH	W/R	BIOS Extension



8.1.5 System BIOS Area (F_0000h-F_FFFFh)

This area is a single 64 kB segment (000F_0000h – 000F_FFFFh). This segment can be assigned read and write attributes. It is by default (after reset) Read/Write disabled and cycles are forwarded to DMI. By manipulating the Read/Write attributes, the GMCH can "shadow" BIOS into the main DRAM. When disabled, this segment is not remapped.

Non-snooped accesses from PCI Express or DMI to this region are always sent to DRAM.

Table 8-3. System BIOS Area Memory Segments

Memory Segments	Attributes	Comments
0F0000H - 0FFFFFH	WE RE	BIOS Area

8.1.6 Programmable Attribute Map (PAM) Memory Area Details

The 13 sections from 768 kB to 1 MB comprise what is also known as the PAM Memory Area.

The GMCH does not handle IWB (Implicit Write-Back) cycles targeting DMI. Since all memory residing on DMI should be set as non-cacheable, there normally will not be IWB cycles targeting DMI.

However, DMI becomes the default target for CPU and DMI originated accesses to disabled segments of the PAM region. If the MTRRs covering the PAM regions are set to WB or RC it is possible to get IWB cycles targeting DMI. This may occur for DMI originated cycles to disabled PAM regions.

For example, say that a particular PAM region is set for "Read Disabled" and the MTRR associated with this region is set to WB. A DMI master generates a memory read targeting the PAM region. A snoop is generated on the FSB and the result is an IWB. Since the PAM region is "Read Disabled" the default target for the Memory Read becomes DMI. The IWB associated with this cycle will cause the GMCH to hang.

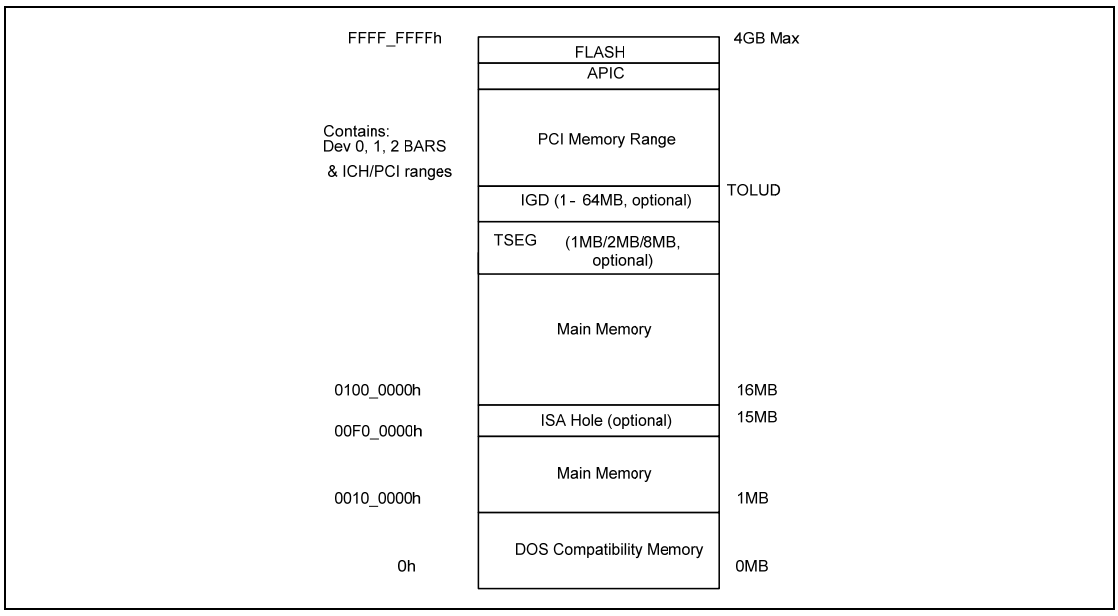
8.2 Main Memory Address Range (1 MB to TOLUD)

This address range extends from 1 MB to the top of physical memory that is permitted to be accessible by the GMCH (as programmed in the TOLUD register). All accesses to addresses within this range will be forwarded by the GMCH to the DRAM unless they fall into the optional TSEG, optional ISA Hole, or optional IGD stolen VGA memory.

The GMCH provides a maximum DRAM address decode space of 4 GB. The GMCH does not remap APIC or PCI Express memory space. This means that as the amount of physical memory populated in the system reaches 4 GB, there will be physical memory that exists yet is non-addressable and therefore unusable by the system.

The GMCH does not limit DRAM address space in hardware.

Figure 8-3. Main Memory Address Range



8.2.1 ISA Hole (15 MB-16 MB)

Legacy ISA based video accelerators originally used this hole. A hole can be created at 15 MB-16 MB as controlled by the fixed hole enable in Device 0 space. Accesses within this hole are forwarded to the DMI. The range of physical DRAM memory disabled by opening the hole is not remapped to the top of the memory – that physical DRAM space is not accessible. This 15 MB-16 MB hole is an optionally enabled ISA hole.



8.2.2 TSEG

TSEG is optionally 1 MB, 2 MB, or 8 MB in size. TSEG is below IGD stolen memory, which is at the top of physical memory. SMM-mode CPU accesses to enabled TSEG access the physical DRAM at the same address. Non-CPU originated accesses are not allowed to SMM space. PCI Express, DMI, and Internal Graphics originated cycles to enabled SMM space are handled as invalid cycle type with reads and writes to location 0 and byte enables turned off for writes. When the extended SMRAM space is enabled, CPU accesses to the TSEG range without SMM attribute or without WB attribute are also forwarded to memory as invalid accesses. Non-SMM-mode Write Back cycles that target TSEG space are completed to DRAM for cache coherency. When SMM is enabled the maximum amount of memory available to the system is equal to the amount of physical DRAM minus the value in the TSEG register which is fixed at 1 MB, 2 MB or 8 MB.

8.2.3 Pre-allocated Memory

Voids of physical addresses that are not accessible as general system memory and reside within system memory address range (< TOLUD) are created for SMM-mode and legacy VGA graphics compatibility. **It is the responsibility of BIOS to properly initialize these regions**. The following table details the location and attributes of the regions. How to enable and disable these ranges are described in the GMCH Control Register Device #0 (GCC).

Table 8-4. Pre-allocated Memory Example for 64-MB Dram, 1-MB VGA, and 1-MB TSEG

Memory Segments	Attributes	Comments
0000_0000h – 03DF_FFFFh	R/W	Available System Memory 62 MB
03E0_0000h – 03EF_FFFFh	SMM Mode Only - CPU Reads	TSEG Address Range & Pre-allocated Memory
03F0_0000h – 03FF_FFFFh	R/W	Pre-allocated Graphics VGA memory. 1MB (or 4/8/16/32/64 MB) when IGD is enabled.

8.3 PCI Express Memory Address Range (TOLUD – 4GB)

This address range, from the top of physical memory to 4 GB (top of addressable memory space supported by the GMCH) is normally mapped via the DMI to PCI.

Exceptions to this mapping include the BAR memory mapped regions, which include: EPBAR, MCHBAR, DMIBAR.

In the PCI Express port, there are two exceptions to this rule:

1. Addresses decoded to the PCI Express Memory Window defined by the MBASE1, MLIMIT1, PMBASE1, and PMLIMIT1 registers are mapped to PCI Express.
2. Addresses decoded to PCI Express Configuration Space are mapped based on Bus, Device, and Function number. (PCIEXBAR range).

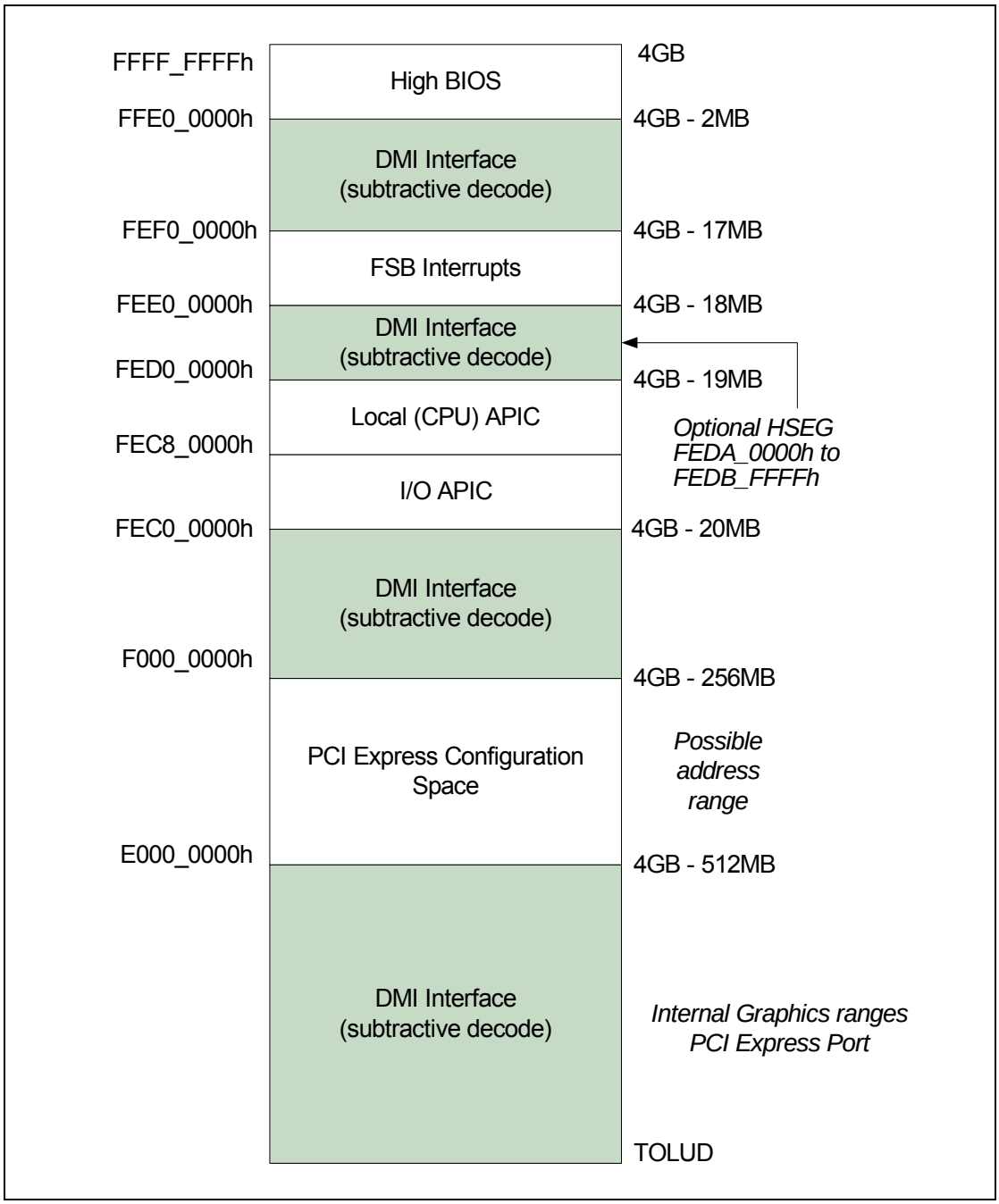
Note: AGP Aperture no longer exists with PCI Express.

In an internal graphics configuration, there are three exceptions to this rule:

3. Addresses decoded to the Graphics Memory Range. (GMADR range)
4. Addresses decoded to the Graphics Translation Table range (GTTADR range).
5. Addresses decoded to the Memory Mapped Range of the Internal Graphics Device (MMADR range). There is a MMADR range for device 2 function 0 and a MMADR range for device 2 function 1. Both ranges are forwarded to the internal graphics device.

Note: The exceptions listed above for internal graphics and the PCI Express ports MUST NOT overlap with APCI Configuration Space, FSB Interrupt Space and High BIOS Address Range.

Figure 8-4. PCI Express Memory Address Range



8.3.1 APIC Configuration Space (FEC0_0000h-FECF_FFFFh)

This range is reserved for APIC configuration space which includes the default I/O APIC configuration space from FEC0_0000h to FEC7_0FFFh. The default Local (CPU) APIC configuration space goes from FEC8_0000h to FECF_FFFFh.

CPU accesses to the Local APIC configuration space do not result in external bus activity since the Local APIC configuration space is internal to the CPU. However, an MTRR must be programmed to make the Local APIC range uncacheable (UC). The Local APIC base address in each CPU should be relocated to the FEC0_0000h (4 GB-20 MB) to FECF_FFFFh range so that one MTRR can be programmed to 64 kB for the Local and I/O APICs. The I/O APIC(s) usually reside in the ICH portion of the chip set or as a stand-alone component(s).

I/O APIC units will be located beginning at the default address FEC0_0000h. The first I/O APIC will be located at FEC0_0000h. Each I/O APIC unit is located at FEC0_x000h where *x* is I/O APIC unit number 0 through F(hex). This address range will normally be mapped to DMI.

Note: There is no provision to support an I/O APIC device on PCI Express.

8.3.2 HSEG (FEDA_0000h-FEDB_FFFFh)

This optional segment from FEDA_0000h to FEDB_FFFFh provides a remapping window to SMM memory. It is sometimes called the High SMM memory space. SMM-mode CPU accesses to the optionally enabled HSEG are remapped to 000A_0000h - 000B_FFFFh. Non-SMM mode CPU accesses to enabled HSEG are considered invalid and are terminated immediately on the FSB. The exceptions to this rule are Non-SMM mode Write Back cycles which are remapped to SMM space to maintain cache coherency. PCI Express and DMI originated cycles to enabled SMM space are not allowed. Physical DRAM behind the HSEG transaction address is not remapped and is not accessible. All Cacheline writes with WB attribute or implicit write backs to the HSEG range are completed to DRAM like an SMM cycle.

8.3.3 FSB Interrupt Memory Space (FEE0_0000-FEEF_FFFF)

The FSB Interrupt space is the address used to deliver interrupts to the FSB. Any device on PCI Express or DMI may issue a Memory Write to 0FEEx_xxxxh. The GMCH will forward this Memory Write along with the data to the FSB as an Interrupt Message Transaction. The GMCH terminates the FSB transaction by providing the response and asserting HTRDY#. This Memory Write cycle does not go to DRAM.

8.3.4 High BIOS Area

The top 2 MB (FFE0_0000h -FFFF_FFFFh) of the PCI Memory Address Range is reserved for System BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS. The CPU begins execution from the High BIOS after reset. This region is mapped to DMI so that the upper subset of this region aliases to the 16 MB-256 kB range. The actual address space required for the BIOS is less than 2 MB but the minimum CPU MTRR range for this region is 2 MB so that full 2 MB must be considered.

8.4 PCI Express Configuration Address Space

There is a Device 0 register (PCIEXBAR), that defines the base address for the 256-MB block of addresses below top of addressable memory (currently 4 GB) for the configuration space associated with all devices and functions that are potentially a part of the PCI Express root complex hierarchy. This range will be aligned to a 256-MB boundary. BIOS must assign this address range such that it will not conflict with any other address ranges.

See the configuration portion of this document for more details.

8.4.1 PCI Express Graphics Attach

The GMCH can be programmed to direct memory accesses to the PCI Express interface when addresses are within either of two ranges specified via registers in GMCH's Device #1 configuration space.

- The first range is controlled via the Memory Base Register (MBASE) and Memory Limit Register (MLIMIT) registers.
- The second range is controlled via the Prefetchable Memory Base (PMBASE) and Prefetchable Memory Limit (PMLIMIT) registers.

The GMCH positively decodes memory accesses to PCI Express memory address space as defined by the following equations:

Memory_Base_Address ≤ Address ≤ Memory_Limit_Address

Prefetchable_Memory_Base_Address ≤ Address ≤ Prefetchable_Memory_Limit_Address

It is essential to support a separate Prefetchable range in order to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining.

Note that the GMCH Device #1 memory range registers described above are used to allocate memory address space for any PCI Express devices sitting on PCI Express that require such a window.

The PCICMD1 register can override the routing of memory accesses to PCI Express. In other words, the memory access enable bit must be set in the device 1 PCICMD1 register to enable the memory base/limit and prefetchable base/limit windows.

8.4.2 AGP DRAM Graphics Aperture

Unlike AGP, PCI Express has no concept of aperture for PCI Express devices. As a result, there is no need to translate addresses from PCI Express. Therefore, the GMCH has no APBASE and APSIZE registers.

8.5 Graphics Memory Address Ranges (Intel Integrated Graphics Chipsets Only)

The GMCH can be programmed to direct memory accesses to IGD when addresses are within any of three ranges specified via registers in GMCH's Device #2 configuration space.

- The Memory Map Base Register (MMADR) is used to access graphics control registers.
- The Graphics Memory Aperture Base Register (GMADR) is used to access graphics memory allocated via the graphics translation table.
- The Graphics Translation Table Base Register (GTTADR) is used to access the translation table.

Normally these ranges will reside above the Top-of-Main-DRAM and below High BIOS and APIC address ranges. They normally reside above the top of memory (TOLUD) so they do not steal any physical DRAM memory space.

GMADR is a Prefetchable range in order to apply USWC attribute (from the processor point of view) to that range. The USWC attribute is used by the processor for write combining.

8.6 System Management Mode (SMM)

System Management Mode uses main memory for System Management RAM (SMM RAM). The GMCH supports: Compatible SMRAM (C_SMRAM), High Segment (HSEG), and Top of Memory Segment (TSEG). System Management RAM space provides a memory area that is available for the SMI handlers and code and data storage. This memory resource is normally hidden from the system OS so that the processor has immediate access to this memory space upon entry to SMM. GMCH provides three SMRAM options:

- Below 1-MB option that supports compatible SMI handlers.
- Above 1-MB option that allows new SMI handlers to execute with write-back cacheable SMRAM.
- Optional TSEG area of 1 MB, 2 MB, or 8 MB in size. The TSEG area lies below IGD stolen memory.

The above 1-MB solutions require changes to compatible SMRAM handlers code to properly execute above 1 MB.

Note: DMI and PCI Express masters are not allowed to access the SMM space.

8.6.1 SMM Space Definition

SMM space is defined by its **addressed** SMM space and its DRAM SMM space. The addressed SMM space is defined as the range of bus addresses used by the CPU to access SMM space. DRAM SMM space is defined as the range of physical DRAM memory locations containing the SMM code. SMM space can be accessed at one of three transaction address ranges: Compatible, High and TSEG.

The Compatible and TSEG SMM space is not remapped and therefore the addressed and DRAM SMM space is the same address range. Since the High SMM space is remapped the addressed and DRAM SMM space are different address ranges. Note that the High DRAM space is the same as the Compatible Transaction Address space. The table below describes three unique address ranges:

- Compatible Transaction Address (Adr C)
- High Transaction Address (Adr H)
- TSEG Transaction Address (Adr T)

These abbreviations are used later in the table describing SMM Space Transaction Handling.

Table 8-5. SMM Space Definition Summary

SMM Space Enabled	Transaction Address Space	DRAM Space (DRAM)
Compatible (C)	000A_0000h to 000B_FFFFh	000A_0000h to 000B_FFFFh
High (H)	FEDA_0000h to FEDB_FFFFh	000A_0000h to 000B_FFFFh
TSEG (T)	(TOLUD-STOLEN-TSEG) to TOLUD-STOLEN	(TOLUD-STOLEN-TSEG) to TOLUD-STOLEN

8.7 SMM Space Restrictions

If any of the following conditions are violated, the results of SMM accesses are unpredictable and may cause the system to hang:

- The Compatible SMM space **must not** be set-up as cacheable.
- High or TSEG SMM transaction address space **must not** overlap address space assigned to system DRAM, or to any “PCI” devices (including DMI, PCI Express, and graphics devices). This is a BIOS responsibility.
- Both D_OPEN and D_CLOSE **must not** be set to 1 at the same time.
- When TSEG SMM space is enabled, the TSEG space **must not** be reported to the OS as available DRAM. This is a BIOS responsibility.
- Any address translated through the GMADR must not target DRAM from A_0000-F_FFFF.

8.7.1 SMM Space Combinations

When High SMM is enabled (G_SMRAME=1 and H_SMRAM_EN=1) the Compatible SMM space is effectively disabled. CPU originated accesses to the Compatible SMM space are forwarded to PCI Express if VGAEN=1 (also depends on MDAP), otherwise they are forwarded to the DMI. PCI Express and DMI originated accesses are **never** allowed to access SMM space.

Table 8-6. SMM Space Table

Global Enable G_SMRAME	High Enable H_SMRAM_EN	TSEG Enable TSEG_EN	Compatible (C) Range	High (H) Range	TSEG (T) Range
0	X	X	Disable	Disable	Disable
1	0	0	Enable	Disable	Disable
1	0	1	Enable	Disable	Enable
1	1	0	Disabled	Enable	Disable
1	1	1	Disabled	Enable	Enable

8.7.2 SMM Control Combinations

The G_SMRAME bit provides a global enable for all SMM memory. The D_OPEN bit allows software to write to the SMM ranges without being in SMM mode. BIOS software can use this bit to initialize SMM code at powerup. The D_LCK bit limits the SMM range access to only SMM mode accesses. The D_CLS bit causes SMM data accesses to be forwarded to the DMI or PCI Express. The SMM software can use this bit to write to video memory while running SMM code out of DRAM.

Table 8-7. SMM Control Table

G_SMRAME	D_LCK	D_CLS	D_OPEN	CPU in SMM Mode	SMM Code Access	SMM Data Access
0	x	X	x	x	Disable	Disable
1	0	X	0	0	Disable	Disable
1	0	0	0	1	Enable	Enable
1	0	0	1	x	Enable	Enable
1	0	1	0	1	Enable	Disable
1	0	1	1	x	Invalid	Invalid
1	1	X	x	0	Disable	Disable
1	1	0	x	1	Enable	Enable
1	1	1	x	1	Enable	Disable

8.7.3 SMM Space Decode and Transaction Handling

Only the CPU is allowed to access SMM space. PCI Express and DMI originated transactions are not allowed to SMM space.

8.7.4 CPU WB Transaction to an Enabled SMM Address Space

CPU Writeback transactions (REQ[1]# = 0) to enabled SMM address space must be written to the associated SMM DRAM even though D_OPEN=0 and the transaction is not performed in SMM mode. This ensures SMM space cache coherency when cacheable extended SMM space is used.

8.8 Memory Shadowing

Any block of memory that can be designated as read-only or write-only can be “shadowed” into GMCH DRAM memory. Typically this is done to allow ROM code to execute more rapidly out of main DRAM. ROM is used as read-only during the copy process while DRAM at the same time is designated write-only. After copying, the DRAM is designated read-only so that ROM is shadowed. CPU bus transactions are routed accordingly.

8.9 I/O Address Space

The GMCH does not support the existence of any other I/O devices beside itself on the CPU bus. The GMCH generates either DMI or PCI Express bus cycles for all CPU I/O accesses that it does not claim. Within the host bridge the GMCH contains two internal registers in the CPU I/O space, Configuration Address Register (CONFIG_ADDRESS) and the Configuration Data Register (CONFIG_DATA). These locations are used to implement a configuration space access mechanism.

The CPU allows 64 k+3 bytes to be addressed within the I/O space. The GMCH propagates the CPU I/O address without any translation on to the destination bus and therefore provides addressability for 64 k+3 byte locations. Note that the upper three locations can be accessed only during I/O address wrap-around when CPU bus HAB_16 address signal is asserted. HAB_16 is asserted on the CPU bus whenever an I/O access is made to 4 bytes from address 0FFFDh, 0FFFEh, or 0FFFFh. HAB_16 is also asserted when an I/O access is made to 2 bytes from address 0FFFFh.

A set of I/O accesses (other than ones used for configuration space access) are consumed by the internal graphics device if it is enabled. The mechanisms for internal graphics I/O decode and the associated control is explained later.

The I/O accesses (other than ones used for configuration space access) are forwarded normally to the DMI bus unless they fall within the PCI Express I/O address range as defined by the mechanisms explained below. I/O writes are NOT posted. Memory writes to ICH or PCI Express are posted. The PCICMD1 register can disable the routing of I/O cycles to PCI Express.

The GMCH responds to I/O cycles initiated on PCI Express or DMI with a UR status. Upstream I/O cycles and configuration cycles should never occur. If one does occur, the request will route as a read to memory address 0h so a completion is naturally generated (whether the original request was a read or write). The transaction will complete with a UR completion status.

For Intel Pentium M Processor with 2 MBL2 Cache processor, I/O reads that lie within 8-byte boundaries but cross 4-byte boundaries are issued from the CPU as 1 transaction. The GMCH will break this into two separate transactions. This has not been done on previous chipsets. I/O writes that lie within 8-byte boundaries but cross 4-byte boundaries are assumed to be split into two transactions by the CPU.

8.9.1 PCI Express I/O Address Mapping

The GMCH can be programmed to direct non-memory (I/O) accesses to the PCI Express bus interface when CPU initiated I/O cycle addresses are within the PCI Express I/O address range. This range is controlled via the I/O Base Address (IOBASE) and I/O Limit Address (IOLIMIT) registers in GMCH Device #1 configuration space.

8.10 GMCH Decode Rules and Cross-Bridge Address Mapping

VGAA = 000A_0000 – 000A_FFFF
MDA = 000B_0000 – 000B_7FFF
VGAB = 000B_8000 – 000B_FFFF

MAINMEM = 0100_0000 to TOLUD

8.10.1 Legacy VGA and I/O Range Decode Rules

The legacy 128 kB VGA memory range 000A_0000h-000B_FFFFh can be mapped to IGD (Device #2), to PCI Express (Device #1), and/or to the DMI depending on the programming of the VGA steering bits. Priority for VGA mapping is constant in that the GMCH always decodes internally mapped devices first. Internal to the GMCH, decode precedence is always given to IGD. The GMCH always positively decodes internally mapped devices, namely the IGD and PCI Express. Subsequent decoding of regions mapped to PCI Express or the DMI depends on the Legacy VGA configurations bits (VGA Enable and MDAP).

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9 Host Interface

9.1 FSB Source Synchronous Transfers

The GMCH supports the Intel Pentium M Processor with 2 MBL2 Cache processor subset of the Enhanced Mode Scaleable Bus. The cache line size is 64 bytes. Source synchronous transfer is used for the address and data signals. The address signals are double pumped and a new address can be generated every other bus clock. At 100 MHz and 133 MHz bus clock the address signals run at 200, 266 and 400 MT/s for a maximum address queue rate of 66 M and 100 M addresses/sec. The data is quad pumped and an entire 64B cache line can be transferred in two bus clocks. At 100 MHz and 133 MHz bus clock the data signals run at 400 and 533 for a maximum bandwidth of 3.2, 4.3, and 6.4 GB/s respectively.

9.2 FSB IOQ Depth

The Scalable Bus supports up to 12 simultaneous outstanding transactions.

9.3 FSB OOQ Depth

The GMCH supports only one outstanding deferred transaction on the FSB.

9.4 FSB GTL+ Termination

The GMCH integrates GTL+ termination resistors on die.

9.5 FSB Dynamic Bus Inversion

The GMCH supports Dynamic Bus Inversion (DBI) when driving and when receiving data from the CPU. DBI limits the number of data signals that are driven to a low voltage on each quad pumped data phase. This decreases the worst-case power consumption of the GMCH. HDINV#_3:0 indicate if the corresponding 16 bits of data are inverted on the bus for each quad pumped data phase:

HDINVB_3:0	Data Bits
HDINV0#	HD15:0#
HDINV1#	HD31:16#
HDINV2#	HD47:32#
HDINV3#	HD63:48#

Whenever the processor or the GMCH drives data, each 16-bit segment is analyzed. If more than 8 of the 16 signals would normally be driven low on the bus the corresponding HDINV# signal will be asserted and the data will be inverted prior to being driven on the bus. Whenever the CPU or the GMCH receives data it monitors HDINV# [3:0] to determine if the corresponding data segment should be inverted.

9.6 FSB Interrupt Overview

The Intel Pentium M Processor with 2 MBL2 Cache processor supports FSB interrupt delivery. They do **not** support the APIC serial bus interrupt delivery mechanism. Interrupt related messages are encoded on the FSB as “Interrupt Message Transactions”. FSB interrupts may originate from the CPUs on the FSB, or from a downstream device on the DMI or PCI Express Graphics Attach. In the later case, the GMCH drives the “Interrupt Message Transaction” on the FSB.

In the IOxAPIC environment, an interrupt is generated from the IOxAPIC to a CPU in the form of an upstream Memory Write. The ICH contains IOxAPICs, and its interrupts are generated as upstream DMI Memory Writes. Furthermore, the PCI 2.3 specification and PCI Express Specifications define MSI’s (Message Signaled Interrupts) that are also in the form of Memory Writes. A PCI device may generate an interrupt as an MSI cycle on it’s PCI bus instead of asserting a hardware signal to the IOxAPIC. The MSI may be directed to the IOxAPIC. The IOxAPIC in turn generates an interrupt as an upstream DMI Memory Write. Alternatively, the MSI may directly route to the FSB. The target of an MSI is dependent on the address of the interrupt Memory Write. The GMCH forwards upstream DMI and PCI Express Graphics Attach low priority Memory Writes to address 0FEEx_xxxxh to the FSB as “Interrupt Message Transactions”.

The GMCH also broadcasts EOI cycles generated by a CPU downstream to the PCI Express Port and DMI interfaces.

9.7 APIC Cluster Mode support

This is required for backwards compatibility with existing software, including various OS’s. As one example, beginning with Microsoft* Windows* 2000 there is a mode (boot.ini) that allows an end user to enable the use of cluster addressing support of the APIC.

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10 Functional Description

This chapter describes the GMCH interfaces and major functional units

10.1 Host Interface

The GMCH supports the Intel Pentium M Processor with 2 MBL2 Cache processor subset of the Enhanced Mode Scaleable Bus. The cache line size is 64 bytes. Source synchronous transfer is used for the address and data signals. The address signals are double pumped and a new address can be generated every other bus clock. At 100 MHz and 133 MHz bus clock the address signals run at 200, 266 and 400 MT/s for a maximum address queue rate of 66 M and 100 M addresses/sec. The data is quad pumped and an entire 64B cache line can be transferred in two bus clocks. At 100 MHz and 133 MHz bus clock the data signals run at 400 and 533 for a maximum bandwidth of 3.2, 4.3, and 6.4 GB/s respectively.

The Scalable Bus supports up to 12 simultaneous outstanding transactions. The GMCH supports only one outstanding deferred transaction on the FSB.

10.1.1 FSB GTL+ Termination

The GMCH integrates GTL+ termination resistors on die.

10.1.2 FSB Dynamic Bus Inversion

The GMCH supports Dynamic Bus Inversion (DBI) when driving and when receiving data from the CPU. DBI limits the number of data signals that are driven to a low voltage on each quad pumped data phase. This decreases the worst-case power consumption of the GMCH. HDINV#_3:0 indicate if the corresponding 16 bits of data are inverted on the bus for each quad pumped data phase:

HDINVB_3:0	Data Bits
HDINV0#	HD15:0#
HDINV1#	HD31:16#
HDINV2#	HD47:32#
HDINV3#	HD63:48#

Whenever the processor or the GMCH drives data, each 16-bit segment is analyzed. If more than 8 of the 16 signals would normally be driven low on the bus the corresponding HDINV# signal will be asserted and the data will be inverted prior to being driven on the bus. Whenever the CPU or the GMCH receives data it monitors HDINV# [3:0] to determine if the corresponding data segment should be inverted.

10.1.3 APIC Cluster Mode support

This is required for backwards compatibility with existing software, including various OS's. As one example, beginning with Microsoft* Windows* 2000 there is a mode (boot.ini) that allows an end user to enable the use of cluster addressing support of the APIC.

The (G)MCH supports three types of interrupt re-direction:

- Physical
- Flat-Logical
- Clustered-Logical

10.2 System Memory Controller

This section describes the GMCH system memory interface for both DDR memory and DDR2 memory. The GMCH supports both DDR and DDR2 memory and either one or two DIMMs per channel.

The Intel 915GM/GME/PM and Intel 910GML/GMLE GMCH DRAM sub-system supports DDR and DDR2 devices.

The Intel 915GMS GMCH DRAM sub-system support only DDR2 devices.

The Mobile Intel® 915GM/GME/PM Express Chipset supports three memory channel organizations:

- Single Channel configuration for DDR 333 MHz devices
- Dual Channel Asymmetric for DDR2 400/533 MHz devices
- Dual Channel Symmetric for DDR2 400/533 MHz devices

The Mobile Intel 910GML/GMLE Express chipset supports three memory channel organizations:

- Single Channel configuration for DDR 333 MHz devices
- Dual Channel Asymmetric for DDR2 400 MHz devices
- Dual Channel Symmetric for DDR2 400 MHz devices

The Intel 915GMS chipset only supports one memory channel organization:

- Single Channel configuration for DDR2 400 MHz devices

If configured as a single channel system, that channel can have one, two, three, or four ranks populated.

If configured as a dual channel system, each channel can have one or two ranks populated. So in either case there can be a maximum of 4 ranks (2 double sided SO-DIMMs) populated.

Table 10-1. System Memory Organization Support for DDR

DDR						
Tech	Width	Page Size	Banks	Smallest Increments	Largest Increments	Maximum Capacity (2 DS SO-DIMMs)
256 Mb	X8	8 k	4	256 MB	512 MB	1 GB
256 Mb	X16	4 k	4	128 MB	256 MB	512 MB
512 Mb	X8	8 k	4	512 MB	1 GB	2 GB
512 Mb	X16	8 k	4	256 MB	512 MB	1 GB
1 GB	X16	8 k	4	512 MB	1 GB	2 GB

Table 10-2. System Memory Organization Support for DDR2

DDR2						
Tech	Width	Page Size	Banks	Smallest Increments	Largest Increments	Maximum Capacity (2 DS SO-DIMMs)
256 Mb	X8	8 k	4	256 MB	512 MB	1 GB
256 Mb	X16	4 k	4	128 MB	256 MB	512 MB
512 Mb	X8	8k	4	512 MB	1 GB	2 GB
512 Mb	X16	8 k	4	256 MB	512 MB	1 GB
1 GB	X16	8 k	8	512 MB	1 GB	2 GB

Table 10-3. DDR / DDR2 Supported Configurations

Technology	Configuration	# of Row Address Bits	# of Column Address Bits	# of Bank Address Bits	Page Size	Rank Size
256 Mbit	16M X 16	13	9	2	4 k	128 MB
256 Mbit	32M X 8	13	10	2	8 k	256 MB
512 Mbit	32M X 16	13	10	2	8 v	256 MB
512 Mbit	64M X 8	13	11	2	16 k	512 MB
512 Mbit	64M X 8	14	10	2	8 k	512 MB
1 Gbit	64M X 16	14	10	2	8 k	512 MB
1 Gbit	128M X 8	14	11	2	16 k	1 GB
1 Gbit	64M X 16	13	10	3	8 k	512 MB
1 Gbit	128M X 8	14	10	3	8 k	1 GB



10.2.1 Memory Channel Organization Modes

The system memory controller supports three styles of memory organization (Symmetric, Asymmetric and Single Channel) and two modes of operation (DDR and DDR2). Rules for populating SO-DIMM slots are included in this chapter.

10.2.1.1 Interleaved (Symmetric) Mode

This mode provides maximum performance on real applications. Addresses are ping-ponged between the channels, and the switch happens after each cache line (64-byte boundary) if a second request sits behind the first, and that request is to an address on the second channel, that request can be sent before data from the first request has returned. Due to this feature, some progress is made even furthering page conflict scenarios. If two consecutive cache lines are requested, both may be retrieved simultaneously, since they are guaranteed to be on opposite channels. The drawbacks of Symmetric mode are that the system designer must populate both channels of memory so they have equal capacity, but the technology and device width may vary from one channel to the other.

Table 10-4. Sample System Memory Organization with Symmetric Channels

	Channel A population	DRBs in Channel A	Channel B population	DRBs in Channel B
Rank 1	512 MB	1024 MB	512 MB	1024 MB
Rank 0	512 MB	512 MB	512 MB	512 MB

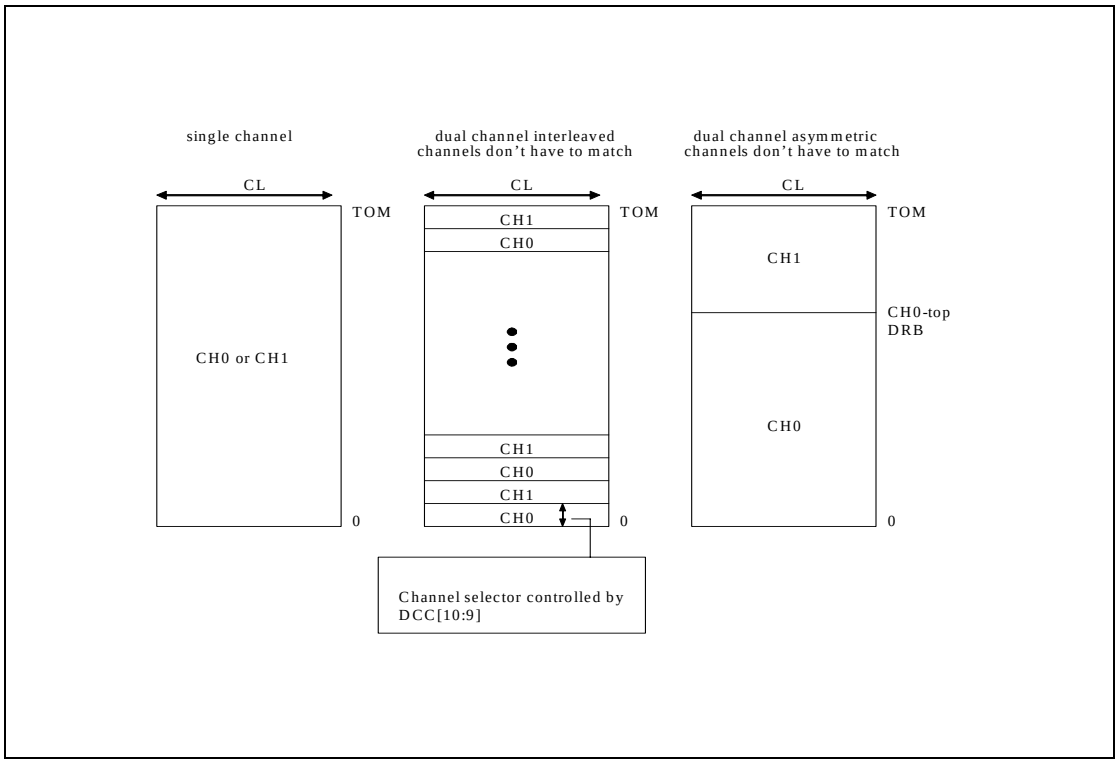
10.2.1.2 Asymmetric Mode

This mode trades performance for system design flexibility. Unlike the previous mode, addresses start in channel A and stay there until the end of the highest rank in channel A, and then addresses continue from the bottom of channel B to the top. Real world applications are unlikely to make requests that alternate between addresses that sit on opposite channels with this memory organization, so in most cases, bandwidth will be limited to that of a single channel. The system designer is free to populate or not to populate any rank on either channel, including either degenerate single channel case.

Table 10-5. Sample System Memory Organization with Asymmetric Channels

	Channel A population	DRBs in Channel A	Channel B population	DRBs in Channel B
Rank 1	1024 MB	1536 MB	512 MB	768 MB
Rank 0	512 MB	512 MB	256 MB	256 MB

Figure 10-1. System Memory Styles



10.2.1.3 DRAM Address Mapping

In the tables below, r indicates a Row address bit, b indicates a bank select bit, and c indicates a column address bit. h indicates a channel select bit, and s indicates that the bit is part of the decode for a chip select (rank select) bit, but since different ranks may use different technologies or organizations, the only way to be sure to which channel and rank an address belongs is to check the DRB register programming. Both s and h are provided for the example of a homogenous population only. Column bit 10 is always used for an AutoPrecharge indication. An asterisk (*) indicates that row address bit 4 will always be driven to 0.

Table 10-6. DRAM Device Configurations –Dual Channel Asymmetric Mode / Single Channel Mode

Technology (Mb)	256X16	256	512	512	512	512	1024	1024	1024	1024
Row bits	13	13	13	13	13	14	14	14	13	14
column bits	9	10	10	11	10	10	10	11	10	10
bank bits	2	2	2	2	2	2	2	2	3	3
width (b)	16	8	16	8	16	8	16	8	16	8
Rows	8192	8192	8192	8192	8192	16384	16384	16384	8192	16384
Columns	512	1024	1024	2048	1024	1024	1024	2048	1024	1024
Banks	4	4	4	4	4	4	4	4	8	8
Page Size (KB)	4	8	8	16	8	8	8	16	8	8
devices per rank	4	8	4	8	4	8	4	8	4	8
Rank Size (MB)	128	256	256	512	256	512	512	1024	512	1024
Depth (M)	16	32	32	64	32	64	64	128	64	128
Addr bits [n:0]	26	27	27	28	27	28	28	29	28	29
available in DDR	yes	yes	yes	yes	no	no	yes	yes	no	no
available in DDR2	yes	yes	no	no	yes	yes	no	no	yes	yes
Host Address bit	Memory Address bit									
31	-	-	-	-	-	-	-	-	-	-
30	-	-	-	-	-	-	-	-	-	-
29	-	-	-	-	-	-	-	r 13	-	r 13
28	-	-	-	r 11	-	r 13	r 13	r 11	r 11	r 11
27	-	r 12	r 12	r 12	r 12	r 12	r 12	r 12	r 12	r 12
26	r 10	r 10	r 10	r 10	r 10	r 10	r 10	r 10	r 10	r 10
25	r 9	r 9	r 9	r 9	r 9	r 9	r 9	r 9	r 9	r 9
24	r 8	r 8	r 8	r 8	r 8	r 8	r 8	r 8	r 8	r 8
23	r 7	r 7	r 7	r 7	r 7	r 7	r 7	r 7	r 7	r 7
22	r 6	r 6	r 6	r 6	r 6	r 6	r 6	r 6	r 6	r 6
21	r 5	r 5	r 5	r 5	r 5	r 5	r 5	r 5	r 5	r 5
20	r 4	r 4	r 4	r 4	r 4	r 4	r 4	r 4	r 4	r 4
19	r 3	r 3	r 3	r 3	r 3	r 3	r 3	r 3	r 3	r 3
18	r 2	r 2	r 2	r 2	r 2	r 2	r 2	r 2	r 2	r 2
17	r 1	r 1	r 1	r 1	r 1	r 1	r 1	r 1	r 1	r 1
16	r 0	r 0	r 0	r 0	r 0	r 0	r 0	r 0	r 0	r 0
15	r 11	r 11	r 11	b 0	r 11	r 11	r 11	b 0	b 0	b 0
14	r 12	b 1	b 1	b 1	b 1	b 1	b 1	b 1	b 1	b 1
13	b 0	b 0	b 0	c 11	b 0	b 0	b 0	c 11	b 2	b 2
12	b 1	c 9	c 9	c 9	c 9	c 9	c 9	c 9	c 9	c 9
11	c 8	c 8	c 8	c 8	c 8	c 8	c 8	c 8	c 8	c 8
10	c 7	c 7	c 7	c 7	c 7	c 7	c 7	c 7	c 7	c 7
9	c 6	c 6	c 6	c 6	c 6	c 6	c 6	c 6	c 6	c 6

Host Address bit	Memory Address bit									
8	c 5	c 5	c 5	c 5	c 5	c 5	c 5	c 5	c 5	c 5
7	c 4	c 4	c 4	c 4	c 4	c 4	c 4	c 4	c 4	c 4
6	c 3	c 3	c 3	c 3	c 3	c 3	c 3	c 3	c 3	c 3
5	c 2	c 2	c 2	c 2	c 2	c 2	c 2	c 2	c 2	c 2
4	c 1	c 1	c 1	c 1	c 1	c 1	c 1	c 1	c 1	c 1
3	c 0	c 0	c 0	c 0	c 0	c 0	c 0	c 0	c 0	c 0

NOTES:
1. b – 'bank' select bit
2. c – 'column' address bit
3. r – 'row' address bit

Table 10-7. DRAM Device Configurations – Dual Channel Symmetric Mode

Technology (Mb)	256	256	512	512	512	512	1024	1024	1024	1024
Row bits	13	13	13	13	13	14	14	14	13	14
column bits	9	10	10	11	10	10	10	11	10	10
bank bits	2	2	2	2	2	2	2	2	3	3
width (b)	16	8	16	8	16	8	16	8	16	8
Rows	8192	8192	8192	8192	8192	16384	16384	16384	8192	16384
Columns	512	1024	1024	2048	1024	1024	1024	2048	1024	1024
Banks	4	4	4	4	4	4	4	4	8	8
Page Size (KB)	4	8	8	16	8	8	8	16	8	8
devices per rank	4	8	4	8	4	8	4	8	4	8
Rank Size (MB)	128	256	256	512	256	512	512	1024	512	1024
Depth (M)	16	32	32	64	32	64	64	128	64	128
Addr bits [n:0]	26	27	27	28	27	28	28	29	28	29
available in DDR	yes	yes	yes	yes	no	no	yes	yes	no	no
available in DDR2	yes	yes	no	no	yes	yes	no	no	yes	yes
Host Address bit	Mem Addr-bit									
31	-	-	-	-	-	-	-	-	-	-
30	-	-	-	-	-	-	-	r 13	-	r 13
29	-	-	-	r 11	-	r 13	r 13	r 11	r 11	r 11
28	-	r 12	r 12	r 12	r 12	r 12	r 12	r 12	r 12	r 12
27	r 10	r 10	r 10	r 10	r 10	r 10	r 10	r 10	r 10	r 10
26	r 9	r 9	r 9	r 9	r 9	r 9	r 9	r 9	r 9	r 9
25	r 8	r 8	r 8	r 8	r 8	r 8	r 8	r 8	r 8	r 8
24	r 7	r 7	r 7	r 7	r 7	r 7	r 7	r 7	r 7	r 7
23	r 6	r 6	r 6	r 6	r 6	r 6	r 6	r 6	r 6	r 6
22	r 5	r 5	r 5	r 5	r 5	r 5	r 5	r 5	r 5	r 5
21	r 4	r 4	r 4	r 4	r 4	r 4	r 4	r 4	r 4	r 4
20	r 3	r 3	r 3	r 3	r 3	r 3	r 3	r 3	r 3	r 3
19	r 2	r 2	r 2	r 2	r 2	r 2	r 2	r 2	r 2	r 2
18	r 1	r 1	r 1	r 1	r 1	r 1	r 1	r 1	r 1	r 1
17	r 0	r 0	r 0	r 0	r 0	r 0	r 0	r 0	r 0	r 0
16	r 11	r 11	r 11	b 0	r 11	r 11	r 11	b 0	b 0	b 0
15	r 12	b 1	b 1	b 1	b 1	b 1	b 1	b 1	b 1	b 1
14	b 0	b 0	b 0	c 11	b 0	b 0	b 0	c 11	b 2	b 2
13	b 1	c 9	c 9	c 9	c 9	c 9	c 9	c 9	c 9	c 9
12	c 8	c 8	c 8	c 8	c 8	c 8	c 8	c 8	c 8	c 8
11	c 7	c 7	c 7	c 7	c 7	c 7	c 7	c 7	c 7	c 7
10	c 6	c 6	c 6	c 6	c 6	c 6	c 6	c 6	c 6	c 6
9	c 5	c 5	c 5	c 5	c 5	c 5	c 5	c 5	c 5	c 5
8	c 4	c 4	c 4	c 4	c 4	c 4	c 4	c 4	c 4	c 4
7	c 3	c 3	c 3	c 3	c 3	c 3	c 3	c 3	c 3	c 3

6	h	h	h	h	h	h	h	h	h	h
5	c 2	c 2	c 2	c 2	c 2	c 2	c 2	c 2	c 2	c 2
4	c 1	c 1	c 1	c 1	c 1	c 1	c 1	c 1	c 1	c 1
3	c 0	c 0	c 0	c 0	c 0	c 0	c 0	c 0	c 0	c 0

NOTES:
1. b – 'bank' select bit
2. c – 'column' address bit
3. h – channel select bit
4. r – 'row' address bit

10.2.2 DRAM Technologies and Organization

All standard 256 Mb, 512 Mb, and 1 Gb technologies and addressing are supported for x16 and x8 devices.

The GMCH supports various page sizes. Page size is individually selected for every rank; 4 kB, 8 kB, and 16 kB for asymmetric, Symmetric, or single channel modes.

The DRAM sub-system supports single or dual channels, 64-bit wide per channel.

A maximum of four ranks (2 double sided SO-DIMMs) populated:

- If configured as a single channel system, that channel can have one, two, three or four ranks populated.
- If configured as a dual channel system, each channel can have one or two ranks populated.

Mixed mode Double-Sided SO-DIMMs (x8 and x16 on the same SO-DIMM) are not supported.

By using 1-Gb technology, the largest memory capacity is 2 GB.

By using 256-Mb technology, the smallest memory capacity is 128 MB (16M x 16b x 4 devices x 1 ranks = 128 MB).

10.2.2.1 Supported SO-DIMM types

DDR

GMCH = supports DDR 200 pin up-buffered SO-DIMM's specified in the JEDEC DDR SO-DIMM specification

- Non ECC, Single Sided, x16 width
- Non ECC, Single Sided, x8 width
- Non ECC, Double Sided, x16 width
- Non ECC, Double Sided, x8 width (stacked)

DDR2

GMCH supports DDR2-SDRAM 200 pin up-buffered SO-DIMM's specified in the JEDEC DDR2 SO-DIMM specification

- Non ECC, Single Sided, x16 width
- Non ECC, Single Sided, x8 width
- Non ECC, Double Sided, x16 width
- Non ECC, Double Sided, x8 width (stacked)

10.2.2.2 Rules for Populating SO-DIMM Slots

In all modes, the frequency of System Memory will be the lowest frequency of all SO-DIMMs in the system, as determined through the SPD registers on the SO-DIMMs.

- In the Single Channel modes, any SO-DIMM slot within the channel may be populated in any order. Either channel may be used. To save power, any unused channel should be powered down.
- In Dual Channel Asymmetric mode, any SO-DIMM slot may be populated in any order.
- In Dual Channel Symmetric mode, any SO-DIMM slot may be populated in any order, but the total memory in each channel must be the same.

10.2.2.3 Pin Connectivity for Single and Dual Channel Modes

Table 10-8. Single Channel Mode Signal Mapping for DDR/DDR2

Single Channel Signal Mapping	
SO-DIMM 0	**SO-DIMM 1**
SM_CK [1:0]	SM_CK [4:3]
SM_CK# [1:0]	SM_CK# [4:3]
SM_CS# [1:0]	SM_CS# [3:2]
SM_CKE [1:0]	SM_CKE [3:2]
SM_ODT[1:0] (DDR2 support only)	SM_ODT [3:2] (DDR2 support only)
SA_BS [2:0]	SB_BS[2:0]
SA_MA[13:0]	SB_MA [13:0]
SA_RAS#	SB_RAS#
SA_CAS#	SB_CAS#
SA_WE#	SB_WE#
SA_DQ [63:0]	
SA_DQS [7:0]	
SA_DQS#[7:0]	
SA_DM[7:0]	

Table 10-9. Dual Channel Mode Signal Mapping for DDR/DDR2

Dual Channel Mode	Channel A	Channel B
	SODIMM A	SODIMM B
SM_CK[1:0]	SM_CK[1:0]	NA
SM_CK[1:0]#	SM_CK[1:0]#	NA
SM_CK[4:3]	NA	SM_CK[4:3]
SM_CK[4:3]#	NA	SM_CK[4:3]#
SM_CS[1:0]#	SM_CS[1:0]#	NA
SM_CKE[1:0]	SM_CKE[1:0]	NA
SM_ODT[1:0] (DDR2 support)	SM_ODT[1:0] (DDR2 support)	NA
SM_CS[3:2]#	NA	SM_CS[3:2]#
SM_CKE[3:2]	NA	SM_CKE[3:2]
SM_ODT[3:2] (DDR2 support)	NA	SM_ODT[3:2] (DDR2 support)

10.2.3 System Memory Configuration Registers Overview

The configuration registers located in the PCI configuration space of the GMCH control the System Memory operation. Following is a brief description of configuration registers used by GMCH for proper operation of the memory subsystem.

DRAM Rank Boundary (CxDRBy)

The x represents a channel, A or B. The y represents a rank, 0 through 1. DRB registers define the upper addresses for a rank of DRAM devices in a channel. When the GMCH is configured in asymmetric mode, each register represents a single rank. When the GMCH is configured in a dual Symmetric mode, each register represents a pair of corresponding ranks in opposing channels. There are four DRB registers for each channel.

DRAM Rank Architecture (CxDRAy)

The x represents a channel, A or B. The y represents a rank, 0 through 1. DRA registers specify the architecture features of each rank of devices in a channel. The only architecture feature specified is page size. When GMCH is configured in asymmetric mode, each DRA represents a single rank in a single channel. When GMCH is configured in a dual-channel lock-step or Symmetric mode, each DRA represents a pair of corresponding ranks in opposing channels. There are four DRA registers per channel. Each requires only 3 bits, so there are two DRAs packed into a byte.

Clock Configuration (CLKCFG)

Specifies DRAM frequency. The same clock frequency will be driven to all SO-DIMMs.

DRAM Timing (CxDRTy)

The x represents a channel, A or B. This register grew too large for a single 32-bit access, so a second register was added, differentiated by y, A or B. The DRT registers define the timing parameters for all devices in a channel. The BIOS programs this register with “least common denominator” values after reading the SPD registers of each SO-DIMM in the channel.

DRAM Control (CxDRCy)

The x represents a channel, A or B. This register grew too large for a single 32 bit access, so a second register was added, differentiated by y, 0 or 1. DRAM refresh mode, rate, and other controls are selected here.

10.2.4 DRAM Clock Generation

The GMCH PLL generates two differential 166 MHz, 200 MHz or 266 MHz clock pairs for every supported SODIMM. There are total of 4 clock pairs driven directly by GMCH to the 2 SO-DIMMs.



10.2.5 DDR2 On-Die Termination

On die termination (ODT) is a feature that allows a DRAM to turn on/off internal termination resistance for each DQ, DM, DQS, and DQS# signal for x8 and x16 configurations via the ODT control signals.

The ODT feature is designed to improve signal integrity of the memory channel by allowing the termination resistance for the DQ, DM, DQS, and DQS# signals to be located inside the DRAM devices themselves instead of on the motherboard. The GMCH drives out the required ODT signals, based on memory configuration and which rank is being written to or read from, to the DRAM devices on a targeted SO-DIMM rank to enable or disable their termination resistance.

10.2.6 DDR2 Off Chip Driver Impedance Calibration

The OCD impedance adjustment mode allows the GMCH to measure and adjust the pull-up and pull-down strength of the DRAM devices. It uses a series of EMRS commands to guide the DRAM through measurement and calibration cycles. This feature is described in more detail in the JEDEC DDR2 device specification.

The algorithm and sequence of the adjustment cycles is handled by software. The GMCH adjusts the DRAM driver impedance by issuing OCD commands to the SO-DIMM and looking at the analog voltage on the DQ lines.

10.2.7 DRAM Power Management

GMCH implements extensive support for power management on the SDRAM interface. GMCH will drive the CKE pins to perform these SDRAM power management operations. During Suspend to RAM (S3) states, the SDRAM are put into self-refresh state to conserve power by asserting the CKE pin. In addition, a “dynamic row power down” function is implemented, by which the SDRAM devices can be put in a power down state when they are idle.

10.2.7.1 Dynamic Row Power Down Operation

GMCH implements CKE control to dynamically put the DRAM devices in a power down state. If dynamic power down is enabled, all ranks are powered up before doing a refresh cycle and all ranks are powered down at the end of refresh.

10.3 PCI Express Interface (Intel® 915GM/915GME/915PM Only)

See system overview chapter in this document for list of PCI Express features. See the PCI Express Specification for further details.

This GMCH is part of a PCI Express root complex. This means it connects a host CPU/memory subsystem to a PCI Express Hierarchy. The control registers for this functionality are located in device #1 configuration space and two Root Complex Register Blocks (RCRBs).

The PCI Express architecture is specified in layers. Compatibility with the PCI addressing model (a load-store architecture with a flat address space) is maintained to ensure that all existing applications and drivers operate unchanged. The PCI Express configuration uses standard mechanisms as defined in the PCI Plug-and-Play specification. The initial speed of 2.5 GHz (250 MHz internally) results in 2.5 Gb/s/direction which provides a 250 MB/s communications channel in each direction (500 MB/s total) that is close to twice the data rate of classic PCI per lane.

10.3.1 Layering Overview

The representation of layers in the PCI Express architecture: the Transaction Layer, the Data Link Layer, and the Physical Layer is to simplify the understanding of the high-level functionality.

PCI Express uses packets to communicate information between components. Packets are formed in the Transaction and Data Link Layers to carry the information from the transmitting component to the receiving component. As the transmitted packets flow through the other layers, they are extended with additional information necessary to handle packets at those layers. At the receiving side the reverse process occurs and packets get transformed from their Physical Layer representation to the Data Link Layer representation and finally (for Transaction Layer Packets) to the form that can be processed by the Transaction Layer of the receiving device.

10.3.2 Transaction Layer

The upper layer of the PCI Express architecture is the Transaction Layer. The Transaction Layer's primary responsibility is the assembly and disassembly of Transaction Layer Packets (TLPs). TLPs are used to communicate transactions, such as read and write, as well as certain types of events. The Transaction Layer also manages flow control of TLPs.

Note: If the (G)MCH receives two back-to-back malformed packets, the second malformed packet is not trapped or logged. The (G)MCH will not log or identify the second malformed packet. However, the 1st malformed TLP is logged, and is considered a Fatal Error. Link behavior is not guaranteed at that point whether a 2nd malformed TLP is detected or not.

10.3.3 Data Link Layer

The middle layer in the PCI Express stack, the Data Link Layer, serves as an intermediate stage between the Transaction Layer and the Physical Layer. Responsibilities of Data Link Layer include link management, error detection, and error correction.

10.3.4 Physical Layer

The Physical Layer includes all circuitry for interface operation, including driver and input buffers, parallel-to-serial and serial-to-parallel conversion, PLL(s), and impedance matching circuitry.

10.4 Intel® Serial Digital Video Output (SDVO) (Intel 915GM/915GME/910GML/910GMLE/915GMS Only)

The SDVO description is located here because it is muxed onto the PCI Express x16 port pins. PCI Express and SDVO simultaneous operation is NOT supported even though SDVO does not require all of the PCI Express lanes. The AC/DC specifications are identical to the PCI Express Graphics interface.

The Intel SDVO port is the second generation of digital video output from compliant Intel GMCHs. The electrical interface is based on the PCI Express interface, though the protocol and timings are completely unique. Whereas PCI Express runs at a fixed frequency, the frequency of the SDVO interface is dependant upon the active display resolution and timing. The port can be dynamically configured in several modes to support display configurations.

Essentially, an SDVO port will transmit display data in a high-speed, serial format across differential AC coupled signals. An SDVO port consists of a sideband differential clock pair and a number of differential data pairs.

10.4.1 Intel® SDVO Capabilities

SDVO ports can support a variety of display types including LVDS, DVI, HDMI, TV-Out, and external CE type devices. The GMCH utilizes an external SDVO device to translate from SDVO protocol and timings to the desired display format and timings. The Internal Graphics controller can have one or two SDVO ports multiplexed on the x16 PCI Express interface. .

The SDVO port defines a two-wire point-to-point communication path between the SDVO device and GMCH. The SDVO Control Clock and Data provide similar functionality to I^2C. However unlike I2C, this interface is intended to be point-to-point (from the GMCH to the SDVO device) and will require the SDVO device to act as a switch and direct traffic from the SDVO Control bus to the appropriate receiver. Additionally, this Control bus will be able to run at faster speeds (up to 1 MHz) than a traditional I2C interface would.

10.4.2 Intel® SDVO Modes

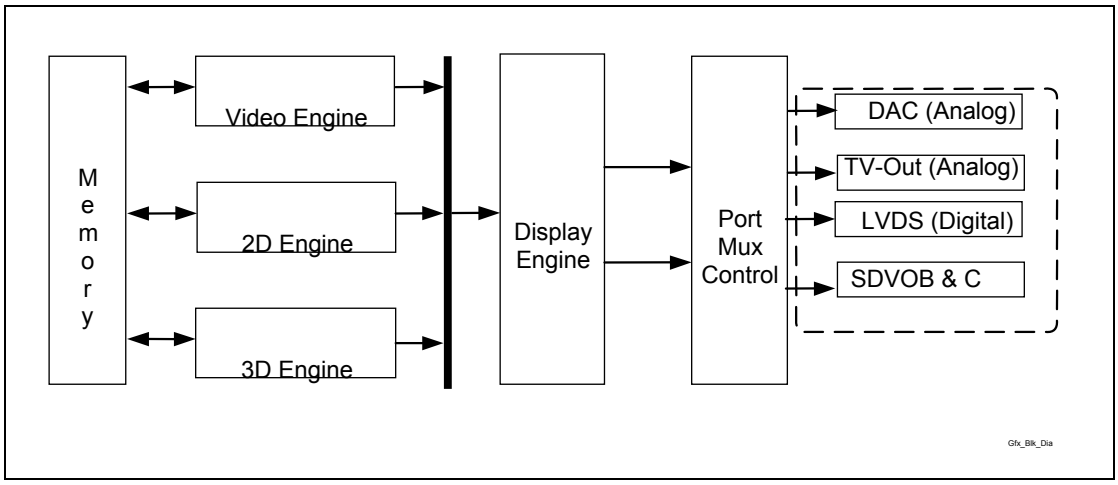
The port can be dynamically configured in several modes:

- Standard – Baseline SDVO functionality. Supports Pixel Rates between 25 and 200 MP/s. Utilizes three data pairs to transfer RGB data.
- Extended – Adds Alpha support to data stream. Supports Pixel Rates between 25 and 200 MP/s. Utilizes four data channels and is only supported on SDVO B. Leverages channel C (SDVO C) Red pair as the Alpha pair for channel B (SDVO B).
- Dual Standard – Utilizes Standard data streams across both SDVO B and SDVO C. Both channels can only run in Standard mode (3 data pairs) and each channel supports Pixel Rates between 25 and 200 MP/s.
- Dual Independent Standard - In Dual Independent Standard mode, each SDVO channel will see a different pixel stream. The data stream across SDVO B will not be the same as the data stream across SDVO C.
- Dual Simultaneous Standard - In Dual Simultaneous Standard mode, both SDVO channels will see the same pixel stream. The data stream across SDVO B will be the same as the data stream across SDVO C. The display timings will be identical, but the transfer timings may not be - i.e. B Clocks and Data may not be perfectly aligned with SDVO C Clock and Data as seen at the SDVO device(s). Since this utilizes just a single data stream, it utilizes a single pixel pipeline within the GMCH.

10.5 Integrated Graphics Controller (Intel® 915GM/915GME/910GML/915GMS Only)

The GMCH provides a highly integrated graphics accelerator and chipset while allowing a flexible integrated system graphics solution.

Figure 10-2. GMCH Graphics Controller Block Diagram



High bandwidth access to data is provided through the graphics and system memory ports. The GMCH can access graphics data located in system memory at 4.2 GB/s – 8.5 GB/s (depending on memory configuration). The GMCH uses Intel's Direct Memory Execution model to fetch textures from system memory.



10.5.1 Integrated Graphics Engine Overview

GMCH's Internal Graphics Device (IGD) contains several types of components.

The GMCH has a 3D/2D Instruction Processing unit to control the graphics engines. The IGD's 3D and 2D engines are fed with data through the memory controller. The output of the engines are processed as surfaces and sent to memory, which are then retrieved and processed by GMCH's display planes.

The IGD graphics engine can be broken down into three components:

- 3D Engine
- 2D Engine
- Video Engine

The entire IGD is fed with data from its memory controller. The graphics performance is directly related to the amount of bandwidth available. If the engines are not receiving data fast enough from the memory controller (e.g., single-channel DDR333), the rest of the IGD will also be affected.

10.6 3D Engine (Intel® 915GM/915GME/910GML/910GMLE/915GMS Only)

The 3D engine of GMCH has been designed with a deep pipelined architecture, where performance is maximized by allowing each stage of the pipeline to simultaneously operate on different primitives or portions of the same primitive. GMCH supports Perspective-Correct Texture Mapping, Multitextures, Bump-Mapping, Cubic Environment Maps, Bilinear, Trilinear and Anisotropic MIP mapped filtering, Gouraud shading, Alpha-blending, Vertex, and Per Pixel Fog and Z/W Buffering.

The 3D pipeline subsystem performs the 3D rendering acceleration. The main blocks of the pipeline are the Setup Engine, Scan Converter, Texture Pipeline, and Raster Pipeline. A typical programming sequence would be to send instructions to set the state of the pipeline followed by rending instructions containing 3D primitive vertex data.

The engines' performance is dependent on the memory bandwidth available. Systems that have more bandwidth available will outperform systems with less bandwidth. The engines' performance is also dependent on the core clock frequency. The higher the frequency, the more data is processed.

10.6.1 Setup Engine

The setup stage of the pipeline takes the input data associated with each vertex of a 3D primitive and computes the various parameters required for scan conversion. In formatting this data, GMCH maintains sub-pixel accuracy.

10.6.1.1 3D Primitives and Data Formats Support

The 3D primitives rendered by GMCH are points, lines, discrete triangles, line strips, triangle strips, triangle fans and polygons. In addition to this, GMCH supports the Microsoft DirectX* Flexible Vertex Format (FVF), which enables the application to specify a variable length of parameter list obviating the need for sending unused information to the hardware. Strips, Fans and Indexed Vertices as well as FVF, improve the vertex rate delivered to the setup engine significantly.

10.6.1.2 Pixel Accurate "Fast" Scissoring and Clipping Operation

The GMCH supports 2D clipping to a scissor rectangle within the drawing window. Objects are clipped to the scissor rectangle, avoiding processing pixels that fall outside the rectangle. The GMCH's clipping and scissoring in hardware reduce the need for software to clip objects, and thus improve performance. During the setup stage, GMCH clips objects to the scissor window.

A scissor rectangle accelerates the clipping process by allowing the driver to clip to a bigger region than the hardware renders to. The scissor rectangle needs to be pixel accurate, and independent of line and point width. GMCH will support a single scissor box rectangle, which can be enabled or disabled. The rectangle is defined as an Inclusive box. Inclusive is defined as "draw the pixel if it is inside the scissor rectangle".

10.6.1.3 Depth Bias

The GMCH supports source Depth Biasing in the Setup Engine. The Depth Bias value is specified in the vertex command packet on a per primitive basis. The value ranges from -1 to 1. The Depth Bias value is added to the z or w value of the vertices. This is used for coplanar polygon priority. If two polygons are to be rendered which are coplanar, due to the inherent precision differences induced by unique x, y and z values, there is no guarantee which polygon will be closer or farther. By using Depth Bias, it is possible to offset the destination z value (compare value) before comparing with the new z value.

10.6.1.4 Backface Culling

As part of the setup, the GMCH discards polygons from further processing, if they are facing away from or towards the user's viewpoint. This operation, referred to as "Back Face Culling" is accomplished based on the "clockwise" or "counter-clockwise" orientation of the vertices on a primitive. This can be enabled or disabled by the driver.

10.6.1.5 Scan Converter

Working on a per-polygon basis, the Scan Converter uses the vertex and edge information is used to identify all pixels affected by features being rendered.

10.6.1.6 Pixel Rasterization Rules

The GMCH supports both OpenGL and D3D pixel rasterization rules to determine whether a pixel is filled by the triangle or line. For both D3D and OpenGL modes, a top-left filling convention for filling geometry will be used. Pixel rasterization rule on rectangle primitive is also supported using the top-left fill convention.

10.6.2 Texture Engine

The GMCH allows an image, pattern, or video to be placed on the surface of a 3D polygon.

The texture processor receives the texture coordinate information from the setup engine and the texture blend information from the scan converter. The texture processor performs texture color or ChromaKey matching, texture filtering (anisotropic, trilinear and bilinear interpolation), and YUV to RGB conversions.



10.6.2.1 Perspective Correct Texture Support

A textured polygon is generated by mapping a 2D texture pattern onto each pixel of the polygon. A texture map is like wallpaper pasted onto the polygon. Since polygons are rendered in perspective, it is important that texture be mapped in perspective as well. Without perspective correction, texture is distorted when an object recedes into the distance.

10.6.2.2 Texture Formats and Storage

The GMCH supports up to 32 bits of color for textures.

10.6.2.3 Texture Decompression

DirectX supports Texture Compression to reduce the bandwidth required to deliver textures. As the textures' average size gets larger with higher color depth and multiple textures become the norm, it becomes increasingly important to provide a mechanism for compressing textures. Texture decompression formats supported include DXT1, DXT2, DXT3, DXT4, DXT5 and FXT1.

10.6.2.4 Texture ChromaKey

ChromaKey describes a method of removing a specific color or range of colors from a texture map before it is applied to an object. For "nearest" texture filter modes, removing a color simply makes those portions of the object transparent (the previous contents of the back buffer show through). For "linear" texture filtering modes, the texture filter is modified if only the non-nearest neighbor texels match the key (range).

10.6.2.5 Anti-Aliasing

Aliasing is one of the artifacts that degrade image quality. In its simplest manifestation, aliasing causes the jagged staircase effects on sloped lines and polygon edges. Another artifact is the moiré patterns which occur as a result of a very small number of pixels available on screen to contain the data of a high resolution texture map. More subtle effects are observed in animation, where very small primitives blink in and out of view.

10.6.2.6 Texture Map Filtering

The GMCH supports many texture mapping modes. Perspective correct mapping is always performed. As the map is fitted across the polygon, the map can be tiled, mirrored in either the U or V directions, or mapped up to the end of the texture and no longer placed on the object (this is known as clamp mode). The way a texture is combined with other object attributes is also definable.

The GMCH supports up to 12 Levels-of-Detail (LODs) ranging in size from 2048x2048 to 1x1 texels. Textures need not be square. Included in the texture processor is a texture cache, which provides efficient MIP mapping.

The GMCH supports seven types of texture filtering:

1. Nearest (Point Filtering): Texel with coordinates nearest to the desired pixel is used. (This is used if only one LOD is present.)
2. Linear (Bilinear Filtering): A weighted average of a 2x2 area of texels surrounding the desired pixel is used. (This is used if only one LOD is present.)
3. Nearest MIP Nearest (Point Filtering): This is used if many LODs are present. The nearest LOD is chosen and the texel with coordinates nearest to the desired pixel is used.
4. Linear MIP Nearest (Bilinear MIP Mapping): This is used if many LODs are present. The nearest LOD is chosen and a weighted average of a 2x2 area of texels surrounding the desired pixel is used (four texels). This is also referred to as Bilinear MIP Mapping.
5. Nearest MIP Linear (Point MIP Mapping): This is used if many LODs are present. Two appropriate LODs are selected and within each LOD the texel with coordinates nearest to the desired pixel is selected. The Final texture value is generated by linear interpolation between the two texels selected from each of the MIP Maps.
6. Linear MIP Linear (Trilinear MIP Mapping): This is used if many LODs are present. Two appropriate LODs are selected and a weighted average of a 2x2 area of texels surrounding the desired pixel in each MIP Map is generated (four texels per MIP Map). The Final texture value is generated by linear interpolation between the two texels generated for each of the MIP Maps. Trilinear MIP Mapping is used minimize the visibility of LOD transitions across the polygon.
7. Anisotropic MIP Nearest (Anisotropic Filtering): This is used if many LODs are present. The nearest LOD-1 level will be determined for each of four sub-samples for the desired pixel. These four sub-samples are then bilinear filtered and averaged together.
8. Both D3D (DirectX 6.0) and OGL (Rev.1.1) allow support for all these filtering modes.

10.6.2.7 Multiple Texture Composition

The GMCH also performs multiple texture composition. This allows the combination of two or greater MIP Maps to produce a new one with new LODs and texture attributes in a single or iterated pass. Flexible vertex format support allows multitexturing because it makes it possible to pass more than one texture in the vertex structure.

10.6.2.8 Bi-Cubic Filter (4x4 Programmable Texture Filter)

A bi-cubic texture filter can be selected instead of the bilinear filter. The implementation is of a 4x4 separable filter with loadable coefficients. A 4x4 filter can be used for providing high-quality up/ down scaling of 2D or 3D rendered images



10.6.2.9 Cubic Environment Mapping

Environment maps allow applications to render scenes with complex lighting and reflections while significantly decreasing CPU load. There are several methods to generate environment maps such as spherical, circular and cubic. The GMCH supports cubic reflection mapping over spherical and circular since it is the best choice to provide real-time environment mapping for complex lighting and reflections.

Cubic Mapping requires a texture map for each of the 6 cube faces. These can be generated by pointing a camera with a 90-degree field-of-view in the appropriate direction. Per-vertex vectors (normal, reflection or refraction) are interpolated across the polygon and the intersection of these vectors with the cube texture faces is calculated. Texel values are then read from the intersection point on the appropriate face and filtered accordingly.

10.6.3 Raster Engine

The Raster Engine is where the color data such as fogging, specular RGB, texture map blending, etc. is processed. The final color of the pixel is calculated and the RGBA value combined with the corresponding components resulting from the Texture Engine. These textured pixels are modified by the specular and fog parameters. These specular highlighted, fogged, textured pixels are color blended with the existing values in the frame buffer. In parallel, stencil, alpha and depth buffer tests are conducted which will determine whether the Frame and Depth buffers will be updated with the new pixel values.

10.6.3.1 Texture Map Blending

Multiple Textures can be blended together in an iterative process and applied to a primitive. The GMCH allows up to four texture coordinates and texture maps to be specified onto the same polygon. Also, the GMCH supports using a texture coordinate set to access multiple texture maps. State variables in multiple texture are bound to texture coordinates, texture map or texture blending.

10.6.3.2 Combining Intrinsic and Specular Color Components

The GMCH allows an independently specified and interpolated “specular RGB” attribute to be added to the post-texture blended pixel color. This feature provides a full RGB specular highlight to be applied to a textured surface, permitting a high quality reflective colored lighting effect not available in devices which apply texture after the lighting components have been combined. If specular-add state variable is disabled, only the resultant colors from the map blending are used. If this state variable is enabled, RGB values from the output of the map blending are added to values for RS, GS, BS on a component by component basis.

10.6.3.3 Color Shading Modes

The Raster Engine supports the flat and Gouraud shading modes. These shading modes are programmed by the appropriate state variables issued through the command stream.

Flat shading is performed by smoothly interpolating the vertex intrinsic color components (Red, Green, Blue), Specular Highlights (R,G,B), Fog, and Alpha to the pixel, where each vertex color has the same value. The setup engine substitutes one of the vertex's attribute values for the other two vertices attribute values thereby creating the correct flat shading terms. This condition is set up by the appropriate state variables issued prior to rendering the primitive.

OpenGL and D3D use a different vertex to select the flat shaded color. This vertex is defined as the "provoking vertex". In the case of strips/fans, after the first triangle, attributes on every vertex that define a primitive are used to select the flat color of the primitive. A state variable is used to select the "flat color" prior to rendering the primitive.

Gouraud shading is performed by smoothly interpolating the vertex intrinsic color components (Red, Green, Blue). Specular Highlights (R,G,B), Fog, and Alpha to the pixel, where each vertex color has a different value.

All the attributes can be selected independently from one of the shading modes by setting the appropriate value state variables.

10.6.3.4 Color Dithering

Color Dithering helps to hide color quantization errors. Color Dithering takes advantage of the human eye's propensity to "average" the colors in a small area. Input color, alpha, and fog components are converted from 8-bit components to 5- or 6- bit component by dithering. Dithering is performed on blended textured pixels. In 32-bit mode, dithering is not performed on the components

10.6.3.5 Vertex and Per Pixel Fogging

Fogging is used to create atmospheric effects such as low visibility conditions in flight simulator- type games. It adds another level of realism to computer-generated scenes. Fog can be used for depth cueing or hiding distant objects. With fog, distant objects can be rendered with fewer details (fewer polygons), thereby improving the rendering speed or frame rate. Fog is simulated by attenuating the color of an object with the fog color as a function of distance. The higher the density (lower visibility for distant objects). There are two ways to implement the fogging technique: per-vertex (linear) fogging and per-pixel (non-linear) fogging. The per-vertex method interpolates the fog value at the vertices of a polygon to determine the fog factor at each pixel within the polygon. This method provides realistic fogging as long as the polygons are small. With large polygons (such as a ground plane depicting an airport runway), the per-vertex technique results in unnatural fogging.

The GMCH supports both types of fog operations, vertex and per pixel or table fog. If fog is disabled, the incoming color intensities are passed unchanged to the destination blend unit.

10.6.3.6 Alpha Blending (Frame Buffer)

Alpha Blending adds the material property of transparency or opacity to an object. Alpha blending combines a source pixel color (RSGSBS) and alpha (AS) component with a destination pixel color (RDGDBD) and alpha (AD) component. For example, this is so that a glass surface on top (source) of a red surface (destination) would allow much of the red base color to show through.

Blending allows the source and destination color values to be multiplied by programmable factors and then combined via a programmable blend function. The combined and independent selection of factors and blend functions for color and alpha are supported.



10.6.3.7 Microsoft Direct X* API and SGI OpenGL Logic Ops

Both APIs provide a mode to use bitwise ops in place of alpha blending. This is used for rubber-banding, i.e., draw a rubber band outline over the scene using an XOR operation. Drawing it again restores the original image without having to do a potentially expensive redraw.

10.6.3.8 Color Buffer Formats: 8-, 16-, or 32-bits per pixel (Destination Alpha)

The Raster Engine will support 8-bit, 16-bit, and 32-bit Color Buffer Formats. The 8-bit format is used to support planar YUV420 format, which used only in Motion Compensation and Arithmetic Stretch format. The bit format of Color and Z will be allowed to mix.

The GMCH supports both double and triple buffering, where one buffer is the primary buffer used for display and one or two are the back buffer(s) used for rendering.

The frame buffer of the GMCH contains at least two hardware buffers—the Front Buffer (display buffer) and the Back Buffer (rendering buffer). While the back buffer may actually coincide with (or be part of) the visible display surface, a separate (screen or window-sized) back buffer is used to permit double-buffered drawing. That is, the image being drawn is not visible until the scene is complete and the back buffer made visible (via an instruction) or copied to the front buffer (via a 2D BLT operation). Rendering to one and displaying from the other remove the possibility of image tearing. This also speeds up the display process over a single buffer. Additionally, triple back buffering is also supported. The instruction set of the GMCH provides a variety of controls for the buffers (e.g., initializing, flip, clear, etc.).

10.6.3.9 Depth Buffer

The Raster Engine will be able to read and write from this buffer and use the data in per fragment operations that determine whether resultant color and depth value of the pixel for the fragment are to be updated or not.

Typical applications for entertainment or visual simulations with exterior scenes require far/near ratios of 1000 to 10000. At 1000, 98% of the range is spent on the first 2% of the depth. This can cause hidden surface artifacts in distant objects, especially when using 16-bit depth buffers. A 24 bit Z-buffer provides 16 million Z-values as opposed to only 64 K with a 16-bit Z buffer. With lower Z-resolution, two distant overlapping objects may be assigned the same Z-value. As a result, the rendering hardware may have a problem resolving the order of the objects, and the object in the back may appear through the object in the front.

By contrast, when W (or eye-relative Z) is used, the buffer bits can be more evenly allocated between the near and far clip planes in world space. The key benefit is that the ratio of far and near is no longer an issue, allowing applications to support a maximum range of miles, yet still get reasonably accurate depth buffering within inches of the eye point.

The GMCH supports a flexible format for the floating-point W buffer, wherein the number of exponent bits is programmable. This allows the driver to determine variable precision as a function of the dynamic range of the W (screen-space Z) parameter.

The selection of depth buffer size is relatively independent of the color buffer. A 16-bit Z/W or 24 bit Z/W buffer can be selected with a 16-bit color buffer. Z buffer is not supported in 8-bit mode.

10.6.3.10 Stencil Buffer

The Raster Engine will provide 8-bit stencil buffer storage in 32-bit mode and the ability to perform stencil testing. Stencil testing controls 3D drawing on a per pixel basis, conditionally eliminating a pixel on the outcome of a comparison between a stencil reference value and the value in the stencil buffer at the location of the source pixel being processed. They are typically used in multipass algorithms to achieve special effects, such as decals, outlining, shadows and constructive solid geometry rendering.

10.6.3.11 Projective Textures

The GMCH will support two, simultaneous projective textures at full rate processing, and four textures at half rate. These textures require three floating point texture coordinates to be included in the Flexible Vertex Format(FVF). Projective textures enable special effects such as projecting spot light textures obliquely onto walls, etc.

10.7 2D Engine (Intel® 915GM/915GME/910GML/910GMLE/915GMS Only)

The GMCH contains BLT functionality, and an extensive set of 2D instructions. To take advantage of the 3D drawing engine's functionality, some BLT functions such as Alpha BLTs, arithmetic (bilinear) stretch BLTs, rotations, transposing pixel maps, limited color space conversion, and DIBs make use of the 3D renderer.

10.7.1 GMCH VGA Registers

The 2D registers are a combination of registers based on the Video Graphics Array (VGA) adapter and others that Intel has added to support graphics modes that have color depths, resolutions, and hardware acceleration features that go beyond the original VGA standard.

10.7.2 2D Functionality

10.7.2.1 Block Level Transfer (BLT) Function

The stretch BLT function can stretch source data in the X and Y directions to a destination larger or smaller than the source. Stretch BLT functionality expands a region of memory into a larger or smaller region using replication and interpolation. The stretch BLT function also provides format conversion and data alignment.



10.7.2.2 Logical 128-bit Fixed BLT and 256-bit Fill Engine

Use of this BLT engine accelerates the Graphical User Interface (GUI) of Microsoft Windows* operating systems. The 128-bit GMCH BLT Engine provides hardware acceleration of block transfers of pixel data for many common Windows operations. The term BLT refers to a block transfer of pixel data between memory locations. The BLT engine can be used for the following:

- Move rectangular blocks of data between memory locations
- Data alignment
- Perform logical operations (raster ops)

The rectangular block of data does not change as it is transferred between memory locations. The allowable memory transfers are between: cacheable system memory and frame buffer memory, frame buffer memory and frame buffer memory, and within system memory. Data to be transferred can consist of regions of memory, patterns, or solid color fills. A pattern will always be 8x8 pixels wide and may be 8, 16, or 32 bits per pixel.

The GMCH BLT engine has the ability to expand monochrome data into a color depth of 8, 16, or 32 bits. BLTs can be either opaque or transparent. Opaque transfers move the data specified to the destination. Transparent transfers compare destination color to source color and write according to the mode of transparency selected.

Data is horizontally and vertically aligned at the destination. If the destination for the BLT overlaps with the source memory location, the GMCH can specify which area in memory to begin the BLT transfer. Hardware is included for all 256 raster operations (Source, Pattern, and Destination) defined by Microsoft, including transparent BLT.

The GMCH has instructions to invoke BLT and stretch BLT operations, permitting software to set up instruction buffers and use batch processing. The GMCH can perform hardware clipping during BLTs.

10.8 Video Engine (Intel® 915GM/915GME/910GML/910GMLE/915GMS Only)

10.8.1 Hardware Motion Compensation

The motion compensation (MC) process consists of reconstructing a new picture by predicting (either forward, backward, or bi-directionally) the resulting pixel colors from one or more reference pictures. The GMCH receives the video stream and implements MC and subsequent steps in hardware. Performing MC in hardware reduces the processor demand of software-based MPEG-2 decoding, and thus improves system performance.

The MC functionality is overloaded onto the texture cache and texture filter. The texture cache is used to typically access the data in the reconstruction of the frames and the filter is used in the actual motion compensation process. To support this overloaded functionality the texture cache additionally supports the following input formats: YUV420 planar.

10.8.2 Sub-Picture Support

Sub-picture is used for two purposes, one is Subtitles for movie captions, etc. (which are superimposed on a main picture), and menus used to provide some visual operation environments the user of a content player.

DVD allows movie subtitles to be recorded as Sub-pictures. On a DVD disc, it is called "Subtitle" because it has been prepared for storing captions. Since the disc can have a maximum of 32 tracks for Subtitles, they can be used for various applications, for example, as Subtitles in different languages or other information to be displayed.

There are two kinds of menus, the system menus and other In-Title Menus. First, the system menus are displayed and operated at startup of or during the playback of the disc or from the stop state. Second, In-Title menus can be programmed as a combination of Sub-picture and Highlight commands to be displayed during playback of the disc.

The GMCH supports sub-picture for DVD and DBS by mixing the two video streams via alpha blending. Unlike color keying, alpha blending provides a softer effect and each pixel that is displayed is a composite between the two video stream pixels. The GMCH can utilize four methods when dealing with sub-pictures. The flexibility enables the GMCH to work with all sub- picture formats.

10.8.3 De-interlacing Support

For display on a progressive computer monitor, interlaced data that has been formatted for display on interlaced monitors (TV), needs to be de-interlaced. The simple approaches to de-interlacing create unwanted display artifacts. More advanced de-interlacing techniques have a large cost associated with them. The compromise solution is to provide a low cost but effective solution and enable both hardware and software based external solutions. Software based solutions are enabled through a high bandwidth transfer to system memory and back.



10.8.3.1 Dynamic Bob and Weave

Interlaced data that originates from a video camera creates two fields that are temporally offset by 1/60 of a second. There are several schemes to de-interlace the video stream: line replication, vertical filtering, field merging and vertical temporal filtering. Field merging takes lines from the previous field and inserts them into the current field to construct the frame – this is known as Weaving. This is the best solution for images with little motion however, showing a frame that consists of the two fields will have serration or feathering of moving edges when there is motion in the scene. Vertical filtering or "Bob" interpolates adjacent lines rather replicating the nearest neighbor. This is the best solution for images with motion however, it will have reduced spatial resolution in areas that have no motion and introduces jaggies. In absence of any other de-interlacing, these form the baseline and are supported by the GMCH.

10.9 Display Interfaces (Intel® 915GM/915GME/910GML/ 910GMLE/915GMS Only)

Note: The Intel 915GME and Intel 910GMLE chipsets do not support the TV-Out display interface.

The display is the defining portion of a graphics controller. The display converts a set of source images or surfaces, combines them and sends them out at the proper timing to an output interface connected to a display device. Along the way, the data can be converted from one format to another, stretched or shrunk, and color corrected or gamma converted.

The GMCH is able to drive a CRT, LCD panel, Analog TV and/or two SDVO ports (muxed with PCI Express) capable of driving an SDVO device. External SDVO devices are capable of driving a standard progressive scan analog monitor with resolutions up to 2048x1536 at 75 Hz. The SDVO ports are capable of driving a variety of TV-Out, TMDS, and LVDS transmitters.

10.9.1 Display Overview

The graphics display can be broken down into three components:

- Display Planes
- Display Pipes
- Display Ports

The display planes are broken down into: primary and secondary display, overlay, sprite, primary and secondary cursor and VGA.

The display pipe consists of the target where the display planes that will be combined meet and a timing generator to set the graphics timing modes. The timing generator determines which time the display occurs.

The display port is the destination for the result of the pipe. The GMCH contains five display ports, two analog (CRT DAC and TV out) and three digital (LVDS, SDVO B and SDVO C). The ports will be explained in more detail later in this chapter.

10.9.2 Planes

The GMCH contains a variety of planes, such as primary and secondary display, overlay, sprite, primary and secondary cursor and VGA. A plane consists of rectangular shaped image that has characteristics such as source, size, position, method, and format. These planes get attached to source surfaces, which are rectangular memory surfaces with a similar set of characteristics. They are also associated with a particular destination pipe.

10.9.2.1 Display Plane

The primary and secondary display plane works in an indexed move, hi-color mode or a true color mode. The true color mode allows for an 8-b alpha channel. One of the primary operations of the display plane is the set mode operation. The set-mode operation occurs when it is desired to enable a display, change the display timing, or source format. The secondary display plane can be used as a primary surface on the secondary display or as a sprite planes on either the primary or secondary display.

10.9.2.2 Cursor A/B Plane

The cursor planes are one of the simplest display planes. The cursors can operate as cursors or as a popup. The cursors can operate in either the alpha blended mode or the AND/XOR mode. These planes are always the top in the Z-order with the other planes. When both cursors are on the same display pipe, cursor A is always above cursor B. With a few exceptions, the cursor plan has a fixed size of 64x64 and a fixed Z-order (top). In legacy modes, cursor can cause the display data below it to be inverted.

10.9.2.3 Cursor Color Formats

Color data can be in an indexed format or a true color format. Indexed data uses the entries in the four entry cursor palette to convert the two-bit index to a true color format before being passed to the blenders. The index can optionally specify that a cursor pixel be transparent or cause an inversion of the pixel value below it or one of two colors from the cursor palette. Blending of YUV or RGB data is only supported with planes that have data of the same format.



10.9.2.4 Popup Cursor

The popup cursor plane is used for control functions in mobile applications. This is not used for typical desktop applications. Either Cursor or cursor B can be used as a popup with exceptions based on restrictions on usage of cursor B

The requirements for the hardware icon

- 64 by 64 pixels 4 colors
- Displayable in all standard and centered VGA modes and all extended modes
- Can be positioned anywhere on the screen
- Flat memory addressing for source (can load images with a single string move instruction)

Only the hardware cursor has a higher Z-order precedence over the hardware icon. Icon should appear over any video windows (full motion video or live video input) but should appear under the hardware cursor if it exists.

Hardware icon memory must be protected from being overwritten by video drivers, video BIOS or the video controller itself. This can be done through software (the video BIOS and drivers are aware of the icon memory and do not use it).

In standard modes (non-VGA) either cursor A or cursor B can be used for a popup with the limitations of cursor B cannot be used in double wide mode. VGA and double wide modes must use cursor A for the popup. Popup on the VGA modes must not use the 32-bpp data format.

10.9.2.5 Overlay Plane

The overlay engine provides a method of merging either video capture data (from an external Video Capture device) or data delivered by the CPU, with the graphics data on the screen. The source data can be mirrored horizontally or vertically or both.

Source/Destination Color Keying/Chroma Keying

Overlay source/destination Chroma Keying enables blending of the overlay with the underlying graphics background. Destination color keying/Chroma Keying can be used to handle occluded portions of the overlay window on a pixel by pixel basis that is actually an underlay. Destination Chroma Keying would only be used for YUV pass through to TV. Destination color keying supports a specific color (8- or 15-bit) mode as well as 32-bit alpha blending.

Source color keying/Chroma Keying is used to handle transparency based on the overlay window on a pixel by pixel basis. This is used when “blue screening” an image to overlay the image on a new background later.

Gamma Correction

Gamma correction is applied to the video signal to compensate for the nonlinear characteristics of the display device and the human eye. Applying the correction at the source for digital data makes the best use of the limited number of bits available for each of the color components. The amount of correction applied is determined by the tube characteristics and is different for NTSC TVs (2.2), PAL TVs (2.8), and SVGA type (1.4-2.8) monitors.

To compensate for overlay color intensity loss due to the non-linear response between display devices, the overlay engine supports independent gamma correction. This allows the overlay data to be converted to linear data or corrected for the display device when not blending.

YUV to RGB Conversion

The format conversion can be bypassed in the case of RGB source data. The format conversion assumes that the YUV data is input in the 4:4:4 format and uses the full range scale.

Maximum Resolution and Frequency

The maximum frequency supported by the overlay logic is 180 MHz. The maximum resolution is dependent on a number of variables.

Deinterlacing Support

For display on a progressive computer monitor, interlaced data that has been formatted for display on interlaced monitors (TV), needs to be de-interlaced. The simple approaches to de-interlacing create unwanted display artifacts. More advanced de-interlacing techniques have a large cost associated with them. The compromise solution is to provide a low cost but effective solution and enable both hardware and software based external solutions. Software based solutions are enabled through a high bandwidth transfer to system memory and back.

10.9.2.6 Dynamic Bob and Weave

Weaving is done by - field merging takes lines from the previous field and inserts them into the current field to construct the frame. This is the best solution for images with little motion however, showing a frame that consists of the two fields will have serration or feathering of moving edges when there is motion in the scene.

Vertical filtering or “Bob” interpolates adjacent lines rather replicating the nearest neighbor. This is the best solution for images with motion. However, it will have reduced spatial resolution in areas that have no motion and may introduce jagged edges. In absence of any other deinterlacing, these form the baseline and are supported by the GMCH.



Scaling Filter and Control

The scaling filter has three vertical taps and five horizontal taps. Arbitrary scaling (per pixel granularity) for any video source (YUV422 or YUV420) format is supported.

The overlay logic can scale an input image up to 1600X1200 with no major degradation in the filter used as long as the maximum frequency limitation is met. Display resolution and refresh rate combinations where the dot clock is greater than the maximum frequency require the overlay to use pixel replication.

10.9.2.7 VGA Plane

The VGA plane is a special plane. It is based on legacy interfaces and provides legacy support for applications that use VGA register interface. VGA only works in indexed display modes. The VGA plane is a special case plane. It operates in several modes and has a set of restrictions on its use. It is not to operate with any other planes active except the pop-up plane.

10.9.3 Display Pipes

The GMCH has two independent display pipes, allowing for support of two independent display streams. The pipe is the target of a set of combined planes (done at the Alpha blender) and a timing generator to setup the display timing graphics modes. The timing generators provide the basic timing information for each of the display pipes.

Pipe A can operate in a single-wide or “double-wide” mode at 2x graphics core clock though they are effectively limited by the perspective display port. The display planes and the cursor plane will provide a “double wide” mode to feed the pipe.

10.9.4 Clock Generator Units (DPLL)

The GMCH provides two DPLL clock generator units provide a stable frequency for driving display pipes. It operates by converting an input reference frequency into an output frequency. The timing generators take their input from internal DPLL devices that are programmable to generate pixel clocks in the range of 25-400 MHz. Accuracy for VESA timing modes is required to be within ± 0.5%.

The DPLL can take a reference frequency from the external reference input (DREF_CLKINN/P), (DREF_SSCCLKINN/P) the TV clock input (TVCLKIN).

10.10 Display Ports (Intel® 915GM/915GME/910GML/ 910GMLE/915GMS Only)

A port is the destination for the result of the pipe. The GMCH has five display ports, two analog and three digital.

- CRT
- LVDS
- TV out (Not supported by the Intel 915GME / Intel 910GMLE)
- SDVO B
- SDVO C

The GMCH has one dedicated CRT display port, one TV out port, one LVDS port, and two SDVO ports. SDVO ports B and C are multiplexed with the PCI Express based Graphics interface and are not available if an external PCI Express based Graphics device is in use or a PCI Express x1 device is used. SDVO Ports B and C can also operate in dual-channel mode, where the data bus is connected to both display ports, allowing a single device to take data at twice the pixel rate.

Table 10-10. Display Port Characteristics

		(Analog)	LVDS		Port B (Digital)	Port C (Digital)
Interface Protocol		RGB DAC	LVDS		sDVO 1.0	sDVO 1.0
SIGNALS	HSYNC	Yes Enable/Polarity	Encoded during blanking codes			
	VSYNC	Yes Enable/Polarity	Encoded during blanking codes			
	BLANK	No	No		Encoded	Encoded
	STALL	No	No		Yes	Yes
	Field	No	No		No	No
	Display_Enable	No	Yes*		Encoded	Encoded
Image Aspect Ratio		Programmable and typically 1.33:1 or 1.78:1				
Pixel Aspect Ratio		Square*	Square			
Voltage		RGB 0.7V p-p	1.2 VDC 300 mV p-p	Scalable 1.x V		
Clock		NA	7x Differential	See sDVO clocking section: Differential		
Max Rate		350 Mpixel	224 MPixel	400 Mpixel	200/400 Mpixel	
Format		Analog RGB	Multiple 18/ 24 bpp	RGB 8:8:8 YUV 4:4:4		
Control Bus		DDC1/DDC2B	Optional DDC	GMBUS		
External Device		No	No	TMDS/LVDS Transmitter /TV Encoder		
Connector		VGA/DVI-I		DVI/CVBS/S-Video/Component/SCART		
Special Functions		Monitor Sense	Power Sequence	Hot Plug Detection	High speed mode	TV Sense SCART WSS
Muxed on PCI Express Based Graphics		No	No		Yes	Yes

NOTE: Single signal software selectable between display enable and Blank#.



10.10.1 Analog Display Port Characteristics

The GMCH's analog port utilizes an integrated 400 MHz RAMDAC that can directly drive a standard progressive scan analog monitor up to a resolution of 2048x1536 pixels with 32-bit color at 75 Hz.

The analog display port provides a RGB signal output along with a HSYNC and VSYNC signal. There is an associated DDC signal pair that is implemented using GPIO pins dedicated to the analog port. The intended target device is for a CRT based monitor with a VGA connector. Display devices such as LCD panels with analog inputs may work satisfactory but no functionality has been added to the signals to enhance that capability.

Table 10-11. Analog Port Characteristics

Signal	Port Characteristic	Support
RGB	Voltage Range	0.7 V p-p only
	Monitor Sense	Analog Compare
	Analog Copy Protection	No
	Sync on Green	No
HSYNC VSYNC	Voltage	2.5 V
	Enable/Disable	Port control
	Polarity adjust	VGA or port control
	Composite Sync Support	No
	Special Flat Panel Sync	No
	Stereo Sync	No
DDC	Voltage	Externally buffered to 5V
	Control	Through DDC interface

10.10.1.1 Integrated RAMDAC

The display function contains a RAM-based Digital-to-Analog Converter (RAMDAC) that transforms the digital data from the graphics and video subsystems to analog data for the CRT monitor. GMCH's integrated 400 MHz RAMDAC supports resolutions up to 2048 x 1536 at 75 Hz. Three, 8-bit DACs provide the R, G, and B signals to the monitor.

10.10.1.2 Sync Signals

HSYNC and VSYNC signals are digital. External level shifting buffers are required. These signals can be polarity adjusted and individually disabled in one of the two possible states. The sync signals should power up disabled in the high state. No composite sync or special flat panel sync support will be included.

10.10.1.3 VESA/VGA Mode

VESA/VGA mode provides compatibility for pre-existing software that set the display mode using the VGA CRTC registers. Timings are generated based on the VGA register values.

10.10.1.4 DDC (Display Data Channel)

DDC is a standard defined by VESA. Its purpose is to allow communication between the host system and display. Both configuration and control information can be exchanged allowing Plug and Play* systems to be realized. Support for DDC 1 and 2 is implemented. The Mobile Intel 915 Express Chipset Family uses the CRTDDCCLK and CRTDDCDATA signals to communicate with the analog monitor. Mobile Intel 915 Express Chipset Family will generate these signals at 2.5 V. External pull-up resistors and level shifting circuitry should be implemented on the board.

The GMCH implements a hardware GMBus controller that can be used to control these signals allowing for transactions speeds up to 400 kHz.

10.10.2 Dedicated TV Out Port

Note: No feature in section 10.10.2 is supported by the Intel 915GME / Intel 910GMLE chipsets.

- Integrated TV-out device supported on Display pipe A and pipe B.
- Three Integrated 10 bit DAC
- NTSC/PAL encoder standard formats supported
- Up to 1024x768 resolution supported for NTSC/PAL
- Multiplexed Output interface:
- Composite Video
- S-Video
- Component Video (YprPb)
- Combination: (Composite & S-Video)
- Tri-level Sync signal
- Macrovision support
- Overscan Scaling Support

10.10.2.1 Connectors

The TV-Out interface support three connector types

- Composite (CVBS)
- S-Video
- Component

10.10.2.2 Composite Video Connector

Composite video is connected through a single RCA type connector. This carries the CVBS signal and does not include audio. Audio is normally associated with the video and comes in a single (for mono) or two RCA connectors (stereo).



10.10.2.3 S-Video Connector

The S-Video signal and connector provide an improved quality video image over the composite image by sending separate luminance and chrominance channels. Cross talk between chrominance and luminance is eliminated and the horizontal resolution is increased due to the elimination of the low pass filter in the luminance path. Both the S-Video 4-pin mini DIN connector and the SCART can support this signal type.

10.10.2.4 Component Analog YUV connector

Newer TVs can be connected to a DVD player through an analog YUV connection. These connectors might be labeled as YUV, Y R-Y B-Y, YCrCb, or Y Pr Pb. Three separate RCA connector/cables are used to make the connection. The 1.0 V Y signal includes a 0.3 V sync signal and the U and V signals are 0.7 V. If WSS information is present, it will be on the Y signal.

10.10.2.5 Content Protection

Content protection will be provided through the external encoder using Macrovision. DVD software must verify the presence of a Macrovision TV encoder before playback continues. Simple attempts to disable the Macrovision operation must be detected.

10.10.3 Dedicated LFP LVDS Port

The GMCH has a dedicated ANSI/TIA/EIA –644-1995 Specification compliant dual channel LFP LVDS interface that can support TFT panel resolutions up to UXGA with a maximum pixel format of 18 bpp, and with SSC supported frequency range from 25 MHz to 112 MHz (single channel/dual channel).

The display pipe selected by the LVDS display port is programmed with the panel timing parameters that are determined by installed panel specifications or read from an onboard EDID ROM. The programmed timing values are then “locked” into the registers to prevent unwanted corruption of the values. From that point on, the display modes are changed by selecting a different source size for that pipe, programming the VGA registers, or selecting a source size and enabling the VGA. The timing signals will remain stable and active through mode changes. These mode changes include VGA to VGA, VGA to HiRes, HiRes to VGA, and HiRes to HiRes.

The transmitter can operate in a variety of modes and supports several data formats. The serializer supports 6-bit or 8-bit color and single or dual channel operating modes. The display stream from the display pipe is sent to the LVDS transmitter port at the dot clock frequency, which is determined by the panel timing requirements. The output of LVDS is running at a fixed multiple of the dot clock frequency, which is determined by the mode of operation; single or dual channel.

Depending on configuration and mode, a single channel can take 18 bits of RGB pixel data plus 3 bits of timing control (HSYNC/VSYNC/DE) and output them on three differential data pair outputs. A dual channel interface converts 36 of color information plus the 3 bits of timing control and outputs it on six or eight sets of differential data outputs.

This display port is normally used in conjunction with the pipe functions of panel scaling and 6-8-bit dither. This display port is also used in conjunction with the panel power sequencing and additional associated functions.

When enabled, the LVDS constant current drivers consume significant power. Individual pairs or sets of pairs can be selected to be powered down when not used. When disabled, individual or sets of pairs will enter a low power state. When the port is disabled all pairs enters a low power mode. The panel power sequencing can be set to override the selected power state of the drivers during power sequencing.

For more details on using the GMCH's LFP LVDS interface for TFT panel support, please refer to the *Common Panel Interface Specification, Rev 1.6* for details on:

10.10.4 LVDS panel support

Table 10-12. LVDS Panel support

LVDS panel	XGA 1024 x 768	SXGA 1280 x 1024	SXGA+ 1400 x 1050	UXGA 1600 x 1200
Intel 915GM	X	X	X	X
Intel 915GMS *	X	X	X	
Intel 910GML	X	X	X	

Note: Intel 915GMS only supports single channel LVDS panel types.

Table 10-13. LVDS Wide Panel support

LVDS panel	WXGA 1280 x 760	WSXGA+ 1600 x 900	WUXGA 1920 x 1200
Intel 915GM	X	X	X
Intel 915GMS *	X		

Note: Intel 915GMS only supports single channel LVDS panel types.

10.10.5 LVDS Interface Signals

LVDS for flat panel is compatible with the ANSI/TIA/EIA-644 specification. This is an electrical standard only defining driver output characteristics and receiver input characteristics. There are two LVDS transmitter channels (channel A and channel B) in the LVDS interface. Each channel consists of 4-data pairs and a clock pair. The interface consists of a total of ten differential signal pairs of which eight are data and two are clocks. The phase locked transmit clock is transmitted in parallel with the data being sent out over the data pairs and over the LVDS clock pair.

Each channel supports transmit clock frequency ranges from 25 MHz to 112 MHz, which provides a throughput of up to 784 Mbps on each data output and up to 112 MP/s on the input. When using both channels, they each operate at the same frequency each carrying a portion of the data. The maximum pixel rate is increased to 224 MP/s but may be limited to less than that due to restrictions elsewhere in the circuit.

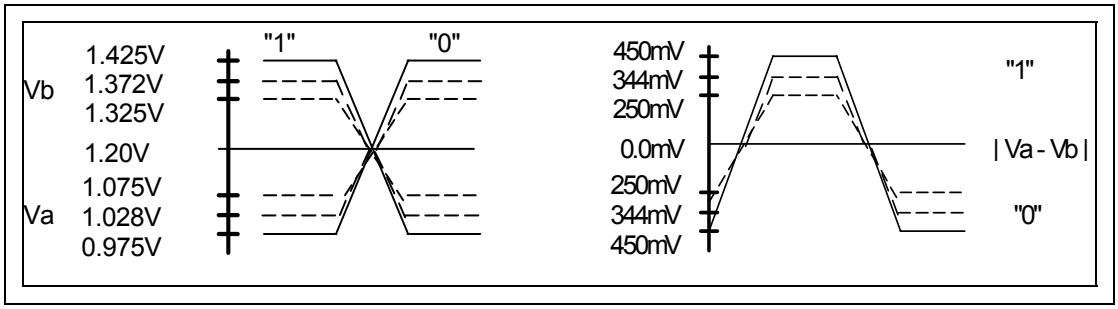
The LVDS Port enable bit enables or disables the entire LVDS interface. When the port is disabled, it will be in a low power state. Once the port is enabled, individual driver pairs will be disabled based on the operating mode. Disabled drivers can be powered down for reduced power consumption or optionally fixed to forced 0's output.

10.10.6 LVDS Data Pairs and Clock Pairs

The LVDS data and clock pairs are identical buffers and differ only in the use defined for that pair. The LVDS data pair is used to transfer pixel data as well as the LCD timing control signals. The pixel bus data to serial data mapping options are specified elsewhere. A single or dual clock pair is used to transfer clocking information to the LVDS receiver. A serial pattern of 1100011 represents one cycle of the clock.

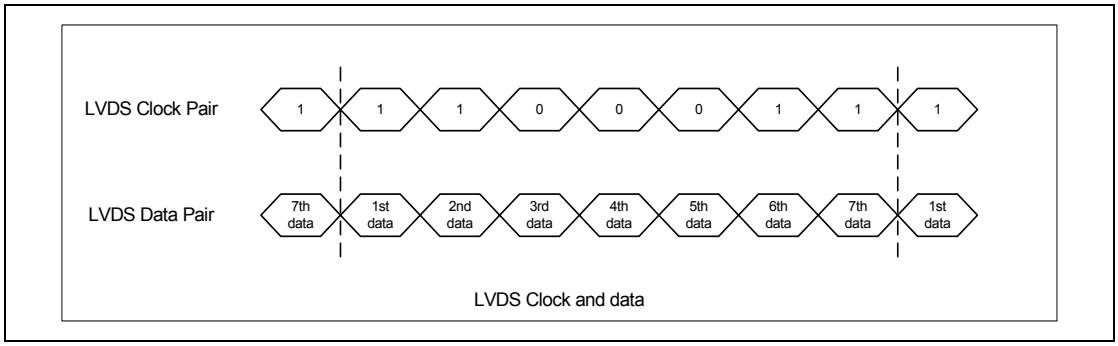
There are two LVDS transmitter channels (channel A and channel B) in the LVDS interface. Each channel contains 1 clock pair and 3-data pair of low voltage differential swing signals. Diagram below shows a pair of LVDS signals and swing voltage.

Figure 10-3. LVDS Swing Voltage



NOTE: 1's and 0's are represented the differential voltage between the pair of signals.

Figure 10-4. LVDS Clock and Data Relationship



10.10.7 LVDS Pair States

The LVDS pairs can be put into one of five states, powered down tri-state, powered down 0 V, common mode, send zeros, or active. When in the active state, several data formats are supported. When in powered down state, the circuit enters a low power state and drives out 0 V or tri-states on both the output pins for the entire channel. The common mode tri-state is both pins of the pair set to the common mode voltage. The common mode state only occurs on B3, A3, or CLKB. These are the signals that optionally get used when driving either 18-bpp panels or dual channel with a single clock. When in the send zeros state, the circuit is powered up but sends only zero for the pixel color data regardless what the actual data is with the clock lines and timing signals sending the normal clock and timing data.

10.10.8 Single Channel versus Dual Channel Mode

Both single channel and dual channel modes are available to allow interfacing to either single or dual channel panel interfaces. This LVDS port can operate in single channel or dual channel mode. Dual channel mode uses twice the number of LVDS pairs and transfers the pixel data at twice the rate of the single channel. In general, one channel will be used for even pixels and the other for odd pixel data. The first pixel of the line is determined by the display enable going active and that pixel will be sent out channel A. All horizontal timings for active, sync, and blank will be limited to be on two pixel boundaries in the two channel modes.

10.10.9 LVDS Channel Skew

When in dual channel mode, the two channels must meet the panel requirements with respect to the inter channel skew.

10.10.10 LVDS PLL

The Display PLL is used to synthesize the clocks that control transmission of the data across the LVDS interface. The three operations that are controlled are the pixel rate, the load rate, and the IO shift rate. These are synchronized to each other and have specific ratios based on single channel or dual channel mode. If the pixel clock is considered the 1x rate, a 7x or 3.5x speed IO_shift clock needed for the high speed serial outputs setting the data rate of the transmitters. The load clock will have either a 1x or .5x ratio to the pixel clock.

10.10.11 SSC Support

The GMCH is designed to tolerate a 0.6%-2.5% down/center spread at a modulation rate range from 30-50 kHz triangle. By using an external SSC clock synthesizer to provide the 66 MHz reference clock into the GMCH Pipe B PLL, spectrally spread 7X, 3.5X, and 1X LVDS clocking is output from GMCH Pipe B PLL.

10.10.12 Panel Power Sequencing

This section provides details for the power sequence timing relationship of the panel power, the backlight enable and the LVDS data timing delivery. In order to meet the panel power timing specification requirements, two signals, PANELVDDEN and PANELBKLTEN are provided to control the timing sequencing function of the panel and the backlight power supplies.

10.10.12.1 Panel Power Sequence States

A defined power sequence is recommended when enabling the panel or disabling the panel. The set of timing parameters can vary from panel to panel vendor, provided that they stay within a predefined range of values. The panel VDD power, the backlight on/off state and the LVDS clock and data lines are all managed by an internal power sequencer.

A requested power-up sequence is only allowed to begin after the power cycle delay time requirement T4 is met.

Figure 10-5. Panel Power Sequencing

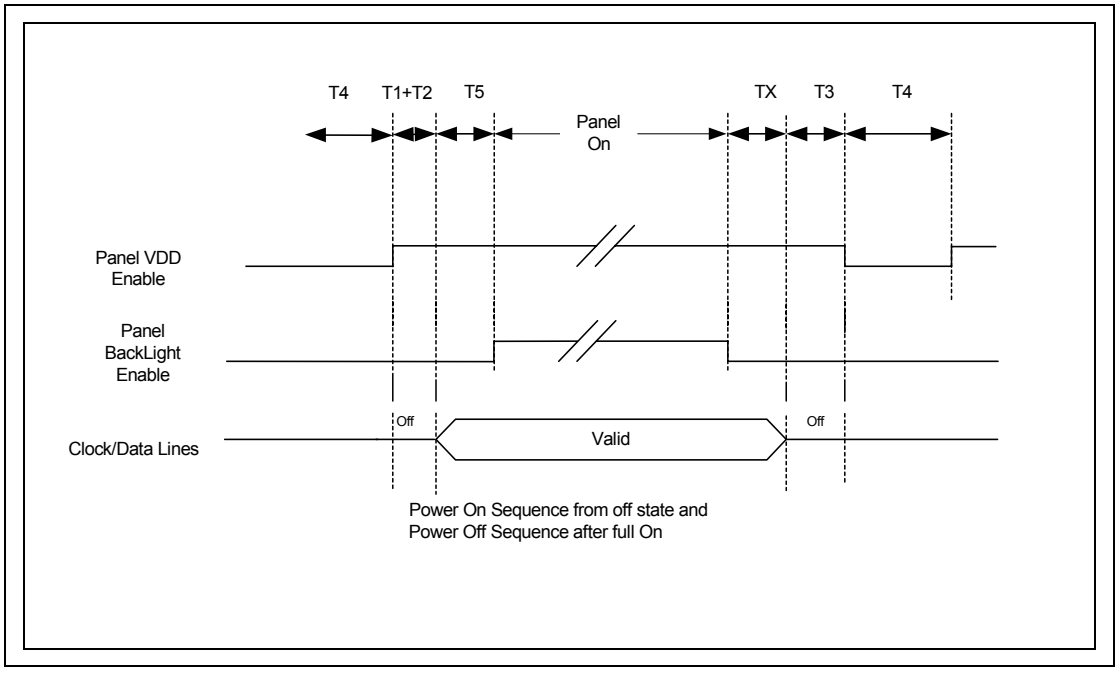


Table 10-14. Panel Power Sequencing Timing Parameters

Name	Panel Power Sequence Timing Parameters			Min	Max	Units
	Spec Name	From	To			
T1+T2	**Vdd On to LVDS Active** Panel Vdd must be on for a minimum time before the LVDS data stream is enabled.	.1 Vdd	LVDS Active	0	60	ms
T5	**Backlight** LVDS data must be enabled for a minimum time before the backlight is turned on.	LVDS Active	Backlight on	200		ms
TX	**Backlight State** Backlight must be disabled for a minimum time before the LVDS data stream is stopped.	Backlight Off	LVDS off	X	X	ms
T3	**LVDS State** Data must be off for a minimum time before the panel VDD is turned off.	LVDS Off	Start power off	0	50	ms
T4	**Power cycle Delay** When panel VDD is turned from On to Off, a minimum wait must be satisfied before the panel VDD is enabled again.	Power Off	Power On Sequence Start	400	X	ms



10.10.12.2 Back Light Inverter Control

The GMCH offers integrated PWM for TFT panel Backlight Inverter brightness control. Other methods of control are specified in the *Common Panel Interface Specification*.

- PWM – based Backlight Brightness Control
- SMBus-based Backlight Brightness Control
- DBL (Display Brightness Link) –to- VDL (Video Data Link) Power Sequencing

10.10.13 SDVO Digital Display Port

The GMCH's SDVO ports are each capable of driving a 200 MP pixel rate. Each port is capable of driving a digital display up to 1600x1200 at 60 Hz. When in dual-channel mode, GMCH can drive a flat panel up to 2048x1536 at 60 Hz or dCRT/HDTV up to 1920x1080 at 85 Hz.

The GMCH is compliant with DVI Specification 1.0. When combined with a DVI compliant external device and connector, the GMCH has a high speed interface to a digital display (e.g., flat panel or digital CRT).

Each port can transmit data according to one or more protocols. The digital ports are connected to an external device that converts one protocol to another. Examples of this are TV encoders, external DACs, LVDS transmitters, and TMDS transmitters. Each display port has control signals that may be used to control, configure and/or determine the capabilities of an external device.

The GMCH has several options for driving digital displays. The GMCH contains two SDVO ports that are multiplexed on the PCI Express based Graphics interface. When an external PCI Express Based Graphics accelerator is not present, the GMCH can use the multiplexed SDVO ports to provide extra digital display options.

he GMCH has the capability to support digital display devices through two SDVO ports muxed with the PCI Express BASED GRAPHICS signals. When an external graphics accelerator is utilized, these SDVO ports are not available.

The shared SDVO ports each support a pixel clock up to 200 MHz and can support a variety of transmission devices. When using a dual-channel external transmitter, it will be possible to pair the two SDVO ports in dual-channel mode to support a single digital display with higher resolutions and refresh rates. In this mode, GMCH is capable of driving pixel clock up to 330 MHz.

SDVOCTRL_DATA is an open-drain signal that will act as a strap during reset to tell the GMCH whether the interface is a PCI Express interface or an SDVO interface. When implementing SDVO device, a pull-up is placed on this line to signal to the GMCH to run in SDVO mode and for proper GMBus operation.

10.10.13.1 TMDS Capabilities

The GMCH is compliant with DVI Specification 1.0. When combined with a DVI compliant external device and connector, the GMCH has a high speed interface to a digital display (e.g., flat panel or digital CRT). When combining the two multiplexed SDVO ports, the GMCH can drive a flat panel up to 2048x1536 or a dCRT/HDTV up to 1920x1080. Flat Panel is a fixed resolution display. The GMCH supports panel fitting in the transmitter, receiver or an external device, but has no native panel fitting capabilities. The GMCH will however, provide unscaled mode where the display is centered on the panel.

10.10.13.2 LVDS Capabilities

The GMCH may use the multiplexed SDVO ports to drive an LVDS transmitter. Flat Panel is a fixed resolution display. The GMCH supports panel fitting in the transmitter, receiver or an external device, but has no native panel fitting capabilities. The GMCH will however, provide unscaled mode where the display is centered on the panel. Mobile Intel® 915 Express Chipset Family supports scaling in the LVDS transmitter through the SDVO stall input pair.

10.10.13.3 TV-Out Capabilities (not supported by the Intel 915GME/Intel 910GMLE)

Although traditional TVs are not digital displays, the GMCH utilizes a digital display channel to communicate with a TV-Out transmitter. For that reason, Mobile Intel® 915 Express Chipset Family considers a TV-Output to be a digital display. GMCH will support NTSC/PAL/SECAM standard definition formats. The GMCH will generate the proper timing for the external encoder. The external encoder is responsible for generation of the proper format signal. Since the multiplexed SDVO interface is

A NTSC/PAL/SECAM display on the TV-out port can be configured to be the boot device. It is necessary to ensure that appropriate BIOS support is provided. If EasyLink is supported in the GMCH, then this mechanism could be used to interrogate the display device.

The TV-out interface on GMCH is addressable as a master device. This allows an external TV encoder device to drive a pixel clock signal on SDVO_TVClk[+/-] that the GMCH uses as a reference frequency. The frequency of this clock is dependent on the output resolution required.

Flicker Filter and Overscan Compensation

The overscan compensation scaling and the flicker filter is done in the external TV encoder chip. Care must be taken to allow for support of TV sets with high performance de-interlacers and progressive scan displays connected to by way of a non-interlaced signal. Timing will be generated with pixel granularity to allow more overscan ratios to be supported.

Direct YUV from Overlay

When source material is in the YUV format and is destined for a device that can take YUV format data in, it is desired to send the data without converting it to RGB. This avoids the truncation errors associated with multiple color conversion steps. The common situation will be that the overlay source data is in the YUV format and will bypass the conversion to RBG as it is sent to the TV port directly.

Sync Lock Support

Sync lock to the TV will be done using the external encoders PLL combined with the display phase detector mechanism. The availability of this feature will be determined which external encoder is in use.

Analog Content Protection

Analog content protection will be provided through the external encoder using Macrovision. DVD software must verify the presence of a Macrovision TV encoder before playback continues. Simple attempts to disable the Macrovision operation must be detected.

Connectors

Target TV connectors support includes the CVBS, S-Video, Component, and SCART connectors. The external TV encoder in use will determine the method of support.

10.10.14 Control Bus

Communication to SDVO registers and monitor DDCs, are accomplished by using the SDVOCTRL_DATA and SDVOCTRL_CLK signals through the SDVO device. These signals run up to 1MHz and connect directly to the SDVO device. The SDVO device is then responsible for routing the DDC and PROM data streams to the appropriate location. Consult SDVO device data sheets for level shifting requirements of these signals.

10.10.15 Intel SDVO Modes

The port can be dynamically configured in several modes:

- Standard – Baseline SDVO functionality. Supports Pixel Rates between 25 and 200 MP/s. Utilizes three data pairs to transfer RGB data.
- Extended – Adds Alpha support to data stream. Supports Pixel Rates between 25 and 200 MP/s. Utilizes four data channels and is only supported on SDVO B. Leverages channel C (SDVO C) Red pair as the Alpha pair for channel B (SDVO B).
- Dual Standard – Utilizes Standard data streams across both SDVO B and SDVO C. Both channels can only run in Standard mode (3 data pairs) and each channel supports Pixel Rates between 25 and 200 MP/s.
 - — Dual Independent Standard - In Dual Independent Standard mode, each SDVO channel will see a different pixel stream. The data stream across SDVO B will not be the same as the data stream across SDVO C.
 - — Dual Simultaneous Standard - In Dual Simultaneous Standard mode, both SDVO channels will see the same pixel stream. The data stream across SDVO B will be the same as the data stream across SDVO C. The display timings will be identical, but the transfer timings may not be - i.e. SDVO B Clocks and Data may not be perfectly aligned with SDVO C Clock and Data as seen at the SDVO device(s). Since this utilizes just a single data stream, it utilizes a single pixel pipeline within the GMCH.

10.11 Multiple Display Configurations

Since the GMCH has several display ports available for its two pipes, it can support up to two different images on different display devices. Timings and resolutions for these two images may be different. Refer to the Mobile Intel 915 Express Chipset Family software PRD for more details on synchronous display support

The GMCH is also incapable of operating in parallel with an external PCI Express graphics device. The GMCH can, however, work in conjunction with a PCI graphics adapter.

10.12 Power Management

Power Management capabilities of the (G)MCH include the following:

10.12.1 Power Management Overview

- ACPI 1.0b and 2.0 compliant power management
- ACPI S0, S3 (Cold and Hot states), S4, S5 states
- CPU States: C0, C1, C2, C3/C4 states
- Internal Graphics Display Device states: D0, D1, D2, D3
- Graphics Display Adapter States: D0, D3
- PCI Express Link States: L0, L0s, L1, L2, L3

10.12.2 ACPI States Overview

GMCH supports the following ACPI states:

10.12.2.1 System

- G0/S0 Full On
- G1/S1 Not supported.
- G1/S2 Not supported.
- G1/S3- Cold Suspend to RAM (STR). Context saved to memory.
- G1/S3-Hot Suspend to RAM (STR). All voltage supplies left on except the CPU Core and FSB VTT.
- G1/S4 Suspend to Disk (STD). All power lost (except wakeup on ICH)
- G2/S5 Soft off. All power lost (except wakeup on ICH). Total reboot.
- G3 Mechanical off. All power (AC and battery) removed from system.



10.12.2.2 CPU

- C0 Full On
- C1 Auto Halt
- C2 Stop Grant.
- C3 Deep Sleep.
- C4 Deeper Sleep.

10.12.2.3 Internal Graphics Display Device Control

- D0 Display active
- D1 Low power state
- D2 Suspend display
- D3 Power off display

10.12.2.4 Internal Graphics Adapter

- D0 Full on, display active
- D3 Hot Graphics clocks off
- D3 Cold Power off

10.12.2.5 PCI Express Link States

- L0 Full on – Active transfer state
- L0s First Active Power Management low power state – Low exit latency
- L1 Lowest Active Power Management– Long exit latency
- L2 Lower link state with power applied – Longer exit latency
- L3 Lowest power state (power off) – Longest exit latency

10.13 Thermal Management

System level thermal management requires comprehending thermal solutions for two domains of operation:

1. Robust Thermal Solution Design: Proper system design should include implementation of a robust thermal solution. The system's thermal solution should be capable of dissipating the platform's TDP power while keeping all components (particularly GMCH, for the purposes of this discussion) below the relevant Tdie_max under the intended usage conditions. Such conditions include ambient air temperature and available airflow inside the notebook.
2. Thermal Failsafe Protection Assistance: As a backup to the implemented thermal solution, the system design should provide a method to provide additional thermal protection for the components of concern (particularly GMCH, for purposes of this discussion). The failsafe assistance mechanism is to help manage components from being damaged by excessive thermal stress under situations in which the implemented thermal solution is inadequate or has failed.

This section covers the thermal failsafe assistance mechanisms that are available for the GMCH and recommends a usage model designed to accomplish the failsafe Protection Assistance.

The GMCH provides two internal thermal sensors, plus hooks for an external thermal sensor mechanism. These can be used for detecting the component temperature and for triggering thermal control within the GMCH. The GMCH has implemented several silicon level thermal management features that can lower both GMCH and DDR power during periods of high activity. These features can help control temperature of the GMCH and DDR and thus help prevent thermally induced component failures. These features include:

- Memory throttling triggering by memory heating
- Memory throttling triggering by GMCH heating
- THRMTRIP# support

10.13.1 Internal Thermal Sensor

The GMCH incorporates two on-die thermal sensors which may be enabled separately. When "tripped" at various values, the thermal sensors may be programmed to cause hardware throttling and/or software interrupts. Hardware throttling includes main memory programmable throttling thresholds. Sensor trip points may also be programmed to be generated various interrupts, including SCI, SMI, SERR, or an internal graphics INTR.



10.13.1.1 Trip Points

There are three programmable temperature trip points for each of the two internal thermal sensors: Catastrophic, Hot, and Auxiliary:

The GMCH can be programmed to generate interrupts when any of these three trip points has been crossed in the upwards direction. In addition, the GMCH can be programmed to enable throttling of the DDR interface when the Catastrophic and/or Hot trip points are crossed in the upwards direction.

- Crossing the Catastrophic trip point may be programmed to generate an interrupt, enable hardware throttling, and immediately shut down the system (via Halt, or via THRMTRIP# assertion).
- Crossing the Hot trip point may be programmed to generate an interrupt and/or enable hardware throttling.
- Crossing the Auxiliary trip point can be programmed to generate an interrupt.

 The current state of all trip points (HOT/CAT/AUX) may be read by software via the Thermal Sensor Status Registers (TSSRs). It is recommended to use Halt or THRMTRIP# assertion on Catastrophic trip. Using an interrupt to initiate shutdown at Catastrophic temperature may be delayed since there is no guaranteed minimum interrupt service latency.

10.13.1.2 Thermometer

The Thermometer Reading Register (TRR) is primarily useful as an indicator of die temperature trending. *The TRR value tends to decrease as the die temperature increases.* Intel currently has no recommended end user usage model for this register. It is provided solely as an indication of temperature trending, for customer system characterization. **Absolute temperature accuracy will vary from part to part. Refer to section** 10.13.4 **for more details on the sensor accuracy (Taccuracy).**

10.13.2 Sample Programming Model

Intel BIOS reference code implements a thermal failsafe mechanism based upon the assumptions stated in the beginning of this chapter. The subsections below describe the algorithms implemented in the reference code.

10.13.2.1 Setting the “Hot” Temperature Trip Point

- Program the Thermal Hot Temperature Setting Register (THTS) as recommended in the latest Mobile Intel® 915 Express Chipset Family BIOS spec and memory reference code.
- Program the Thermal Sensor Control Register (TSC) as recommended in the latest Mobile Intel® 915 Express Chipset Family BIOS spec and memory reference code.
- To enable Error / SMI / SCI / INTR commands for CAT/HOT/AUX trip, set the appropriate bit in TERRCMD / TSMICMD / TSCICMD / TINTRCMD registers. Refer to latest Mobile Intel® 915 Express Chipset Family EDS and BIOS spec update for programming details.

10.13.3 Trip Point Temperature Targets

Table 10-15 below provides recommended trip points based upon the usage model of the thermal sensors as a thermal protection failsafe mechanism. These settings assume that the system's thermal solution has been designed to provide adequate cooling for a TDP power condition and that the settings for the silicon level thermal management are only intended to provide failsafe protection of the part beyond the capabilities of the thermal solution.

Intel's recommended trip point settings take into account the inaccuracy of the internal thermal sensors as described in section 10.13.4 and are intended to cause the GMCH to initiate thermal failsafe control mechanisms at the noted temperatures under the worst case accuracy, Taccuracy. Therefore, in parts which actually exhibit the worst case inaccuracy, failsafe control mechanisms may actually be initiated at a temperature which is Taccuracy below the nominal trip point.

Table 10-15: Recommended Programming for Available Trip Points

Zone	Nominal Trip Points	Recommended action
Catastrophic	$T_{Catastrophic}$ = Tdie,max + 41°C - Taccuracy = 133°C	Halt operation
Hot	$T_{Hot} = T_{die,max} + 3°C + T_{accuracy}$ = 121°C	Initiate throttling
Aux	OEM decision, based on OEM criteria (for example: Taux = Temp at which an auxiliary fan should be turned on)	OEM decision, based on OEM criteria (for example: turn on an auxiliary fan)

Crossing a trip point in either direction may generate several types of interrupts. Each trip point has a register which can be programmed to select the type of interrupt to be generated.

Crossing a trip point may also initiate hardware-based throttling without software intervention.

10.13.4 Thermal Sensor Accuracy

Thermal sensor accuracy, Taccuracy, for GMCH is ± 13 °C for temperature range 80 °C to 133 °C. This value is based on product characterization and is not guaranteed by manufacturing test.

Software has the ability to program the Tcat, Thot, and Taux trip points, but these trip points should be selected with consideration for the thermal sensor accuracy and the quality of the platform thermal solution. Overly conservative (unnecessarily low) temperature settings may unnecessarily degrade performance due to frequent throttling, while overly aggressive (dangerously high) temperature settings may fail to protect the part against permanent thermal damage.

10.13.5 Thermal Throttling Options

The GMCH has two independent mechanisms that cause system memory bandwidth throttling.

The first is GMCH thermal management to ensure that the chipset is operating within thermal limits. The mechanism can be initiated by a thermal sensor (internal or external) trip or by GMCH usage exceeding a programmed threshold via a weighted input averaging filter.

The second is Dram Thermal management to ensure that the dram chips are operating within thermal limits. Throttling can be initiated by dram activity measurement exceeding a programmed threshold.

Another possible usage model targets skin temperature control near memory. Throttling can be initiated by an external thermal sensor trip or by dram activity measurement exceeding a programmed threshold.

10.13.6 THRMTRIP Operation

Assertion of the GMCH's THRMTRIP# (Thermal Trip) indicates the GMCH junction temperature has reached a level beyond which damage may occur. Upon assertion of THRMTRIP#, the GMCH will shut off its internal clocks (thus halting program execution) in an attempt to reduce the GMCH core junction temperature. Once activated, THRMTRIP# remains latched until RSTIN# is asserted. The GMCH THRMTRIP# and CPU THRMMTRIP# signals connects to ICH6-M.

10.14 Clocking

10.14.1 Overview

The GMCH has a total of five PLLs providing many times that many internal clocks. The PLLs are:

- Host PLL – Generates the main core clocks in the host clock domain. Can also be used to generate memory and internal graphics core clocks. Uses the Host clock (HCLKN/HCLKP) as a reference.
- Memory PLL – Can be used to generate memory and internal graphics core clocks, when not generated by the Host PLL. This PLL is not needed in all configurations, but exists to provide more flexible frequency combinations without an unreasonable VCO frequency. Uses the Host clock (HCLKN/HCLKP) as a reference.
- PCI Express PLL – Generates all PCI Express related clocks, including the DMI that connects to the ICH6-M. This PLL uses the 100 MHz (GCLKN/GCLKP) as a reference.
- Display PLL A – Generates the internal clocks for Display A. Uses DREF_CLKIN as a reference.
- Display PLL B – Generates the internal clocks for Display A or Display B. Also may optionally use DREF_SSCCLKIN as a reference for SSC support for LVDS display on pipe B.

10.14.2 GMCH Reference Clocks

Reference Input clocks	Input Frequency	Associated PLL
HCLKP / HCLKN	100 MHz / 133MHz	Host / Memory / Graphics Core
DREF_CLKN / DREF_CLKP	96 MHz / 100 MHz	Display PLL A
DREF_SSCCLKN / DREF_SSCCLKP	96 MHz / 100 MHz	Display PLL B
GCLKP / GCLKN	100 MHz	PCI Express / DMI PLL

10.14.3 Host/Memory/Graphics Core Clock Frequency Support

10.14.3.1 Intel 915GM Host/Memory/Graphics Clock Support

Table 10-16. Intel 915GM Graphics Clock Frequency Support

Host	Memory	Gfx Core Voltage	2D Display core	3D Render core
400 MHz	DDR 333	1.05 V	133, 200	133, 166, 200
533 MHz	DDR 333	1.05 V	133, 190	133, 166, 190
400 MHz	DDR2 400	1.05 V	133, 200	133, 160, 200
533 MHz	DDR2 400	1.05 V	133, 200	133, 160, 200
533 MHz	DDR2 533	1.05 V	133, 200	133, 160, 200
400 MHz	DDR2 400	1.5 V	133, 200,333	133, 160, 200, 333
533 MHz	DDR2 400	1.5 V	133, 200, 333	133, 160, 200, 333
533 MHz	DDR2 533	1.5 V	133, 200, 333	133, 160, 200, 333

10.14.3.2 Intel 915GMS Host/Memory/Graphics Clock Support

Table 10-17. Intel 915GMS Graphics Clock Frequency Support

Host	Memory	Gfx Core Voltage	2D Display core	3D Render core
400 MHz	DDR2 400	1.05 V	133, 200	133, 160

10.14.3.3 Intel 910GML Host/Memory/Graphics Clock Support

Table 10-18. Intel 910GML Graphics Clock Frequency Support

Host	Memory	Gfx Core Voltage	2D Display Core	3D Render Core
400 MHz	DDR 333	1.05 V	133, 200	133, 166
400 MHz	DDR2 400	1.05 V	133, 200	133, 160

§

11 Electrical Characteristics

This chapter contains the absolute maximum electrical ratings, power dissipation values, and DC characteristics.

11.1 Absolute Maximum Ratings

Table 11-1 specifies absolute maximum and minimum ratings. Within functional operating parameters, functionality and long-term reliability can be expected.

At conditions outside functional operating parameters, but within absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. If a device is returned to conditions within functional operating parameters after having been subjected to conditions outside these parameters, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operating parameters.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long-term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time then, when returned to conditions within the functional operating parameters, it will either not function or its reliability will be severely degraded.

Table 11-1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes
T_{die}	Die Temperature under Bias	0	105	°C	1
$T_{storage}$	Storage Temperature	-55	150	°C	2
GMCH Core					
VCC	1.05 V Core Supply Voltage with respect to VSS	-0.3	1.65	V	
VCC	1.5 V Core Supply Voltage with respect to VSS	-0.3	1.65	V	
Host Interface					
VTT (FSB Vccp)	1.05 V AGTL+ buffer DC Input Voltage with respect to VSS	-0.3	1.65	V	
DDR Interface (333 MTs)					
VCCSM	2.5 V DDR System Memory Data Buffers Supply Voltage with respect to VSS	-0.3	4.0	V	
VCCA_SM	1.5 V VCCASM is the Analog power supply for SM data buffers used for DLL & other logic	-0.3	1.65	V	
DDR2 Interface (400 MTs/533 MTs)					
VCCSM	1.8 V DDR2 Supply Voltage with Respect to Vss.	-0.3	4.0	V	
VCCA_SM	1.5 V VCCASM is the Analog power supply for SM data buffers used for DLL & other logic	-0.3	1.65	V	
DMI /PCI Express* Graphics/SDVO Interface					
VCC3G	1.5 V PCI-Express Supply Voltage with respect to VSS	-0.3	1.65	V	
VCCA_3GBG	2.5 V Analog Supply Voltage with respect to VSSA3GBG	-0.3	2.65	V	
CRT DAC Interface (8 bit DAC)					
VCCA_CRTDAC	2.5 V DAC Supply Voltage with respect to VSSA_CRTDAC	-0.3	2.65	V	
VCC_SYNC	2.5 V CRT Sync Supply Voltage	-0.3	2.65	V	
HV CMOS Interface					
VCCHV	2.5 V Supply Voltage with respect to VSS	-0.3	2.65	V	
TV OUT Interface (10 bit DAC)					
VCCD_TVDAC	1.5 V TV Supply	-0.3	1.65	V	
VCCA_TVDACA VCCA_TVDACB VCCA_TVDACC	3.3 V TV Analog Supply	-0.3	3.65	V	
VCCA_TVBG	3.3 V TV Analog Supply	-0.3	3.65	V	
VCCDQ_TVDAC	1.5 V Quiet Supply	-0.3	1.65	V	
LVDS Interface					
VCCD_LVDS	1.5 V LVDS Digital Power Supply	-0.3	1.65	V	
	2.5 V LVDS Data/Clock Transmitter Supply	-0.3	2.65	V	

Symbol	Parameter	Min	Max	Unit	Notes
VCCTX_LVDS	Voltage with respect to VSS				
VCCA_LVDS	2.5 V LVDS Analog Supply voltage with respect to VSS	-0.3	2.65	V	
PLL Analog Power Supplies					
VCCA_HPLL, VCCA_MPLL, VCCD_HMPLL, VCCA_3GPLL, VCCA_DPLLA, VCCA_DPLLB	1.5 V Power Supply for various PLL	-0.3	1.65	V	

NOTES:

1. Functionality is not guaranteed for parts that exceed Tdie temperature above 105 ºC. Tdie is measured at top center of the package. Full performance may be affected if the on-die thermal sensor is enabled.
2. Storage temperature is applicable to storage conditions only. In this scenario, the silicon must not receive a clock, and no pins can be connected to a voltage bias. Storage within these limits will not affect the long-term reliability of the device. This rating applies to the silicon and does not include any tray or packaging. Possible damage to the GMCH may occur if the GMCH temperature exceeds 150 ºC. Intel does not guarantee functionality for parts that have exceeded temperatures above 150 ºC due to spec violation.

11.2 Power Characteristics

Table 11-2. Non-Memory Power Characteristics

Symbol	Parameter	Signal Names	Min	Typ	Max[7]	Unit	Notes
TDP Intel® 915GM/915GME/910GML/910GMLE Intel® 915PM Intel® 915GMS					 6.0 5.5 4.8	W	1, 2
I_{VTT}	VTT Supply Current (1.05v)	VTT			640	mA	
I_{VCC1_05}	1.05 V Core Supply Current (External GFX)	VCC			2600	mA	
I_{VCC1_05}	1.05 V Core Supply Current (Integrated GFX)	VCC			3700	mA	
I_{VCC1_5}	1.5 V Core Supply Current (External GFX)	VCC			4000	mA	
I_{VCC1_5}	1.5 V Core Supply Current (Integrated GFX)	VCC			6750	mA	
I_{VCC3G}	1.5 V PCI Express Supply Current	VCC3G, VCCA_3GPLL			1500	mA	4,6
I_{VCCA_3GBG}	2.5 V PCI Express Analog Supply Current	VCCA_3GBG			0.150	mA	
I_{VCCD_LVDS}	1.5 V LVDS (Digital) Supply Current	VCCD_LVDS			60	mA	
I_{VCCA_LVDS}	2.5 V LVDS (Analog) Supply Current	VCCA_LVDS			10	mA	
I_{VCCTX_LVDS}	2.5 V LVDS (I/O) Supply Current	VCCTX_LVDS			60	mA	
I_{VCCCRT}	2.5 V CRT DAC Supply Current (IvccADAC) 2.5V CRT Sync Supply Current (Ivccsync)	VCCA_CRTDAC VCC_SYNC			68 mA 2 mA		
I_{VCCHV}	2.5 V HV CMOS Supply Current	VCCHV			2	mA	
I_{VCCD_TVDAC}	1.5 V TV Supply Current (Ivcc_TVDAC) 1.5 V TV Quiet Supply Current (IVccQ_TVDAC)	VCCD_TVDAC VCCQ_TVDAC			24	mA	6
$I_{VCCTVDAC}$	3.3 V TV Analog Supply Current (IvccATVDAC) 3.3 V TV Bandgap Supply Current (IvccATVBG)	VCCA_TVBG VCCA_TVDACA VCCA_TVDACB VCCA_TVDACC			120	mA	6
$I_{VCCAHPLL}$	Host PLL Supply Current	VCCA_HPLL			45	mA	

Symbol	Parameter	Signal Names	Min	Typ	Max[7]	Unit	Notes
$I_{VCCADPLLA,B,}$	Display PLLA Supply Current Display PLLB Supply Current	VCCA_DPLLA VCCA_DPLLB			40 40	mA mA	
$I_{VCCAMPLL}$	Memory PLL Supply Current	VCCA_MPLL			45	mA	
$I_{VCCDHMPLL}$	HMPLL Supply Current for Digital Interface	VCCD_HMPLL			150	mA	

NOTES:

1. This spec is the Thermal Design Power and is the estimated maximum possible expected power generated in a component by a realistic application. It is based on extrapolations in both hardware and software technology over the life of the component. It does not represent the expected power generated by a power virus. Studies by Intel indicate that no application will cause thermally significant power dissipation exceeding this specification, although it is possible to concoct higher power synthetic workloads that write but never read. Under realistic read/write conditions, this higher power workload can only be transient and is accounted in the Icc (max) spec. Tdie is measured at the top center of the package.
2. Please contact your Intel Field Representative for latest TDP data.
3. Estimate is only for max current coming through the chipset's supply balls.
4. Rail includes PLL current.
5. Iccmax is determined on a per-interface basis, and all can not happen simultaneously.

Table 11-3. DDR (333 MTs) Power Characteristics

Symbol	Parameter	Min	Type	Max	Unit	Notes
I_{VCCSM} (DDR)	DDR System Memory Interface (2.5 V) Supply Current		1 Channel 2 Channel	1050 2200	mA mA	
I_{SUS_VCCSM} (DDR)	DDR System Memory Interface (2.5 V) Standby Supply Current			N/A	mA	
I_{SMVREF} (DDR)	DDR System Memory Interface Reference Voltage (1.25 V) Supply Current			10	µA/pin	
I_{SUS_SMVREF}	DDR System Memory Interface Reference Voltage (1.25 V) Standby Supply Current			10	µA/pin	
I_{TTRC} (DDR)	DDR System Memory Interface Resistor Compensation Voltage (2.5 V) Supply Current			42	mA	
I_{SUS_TTRC} (DDR)	DDR System Memory Interface Resistor Compensation Voltage (2.5 V) Standby Supply Current			~ 0	µA	
I_{VCCASM}	Memory DLL		1 Channel 2 Channel	125 250	mA	
I_{SUS_VCCASM}	Memory DLL (Standby)		1 Channel 2 Channel	0 0	mA	

Table 11-4. DDR 2 (400 MTs/533 MTs) Power Characteristics

Symbol	Parameter	Min	Type	Max	Unit	Notes
I_{VCCSM} (DDR2)	DDR2 System Memory Interface (1.8 V, 400 MTs) Supply Current		1 Channel 2 Channel	950 1900	mA mA	
I_{VCCSM} (DDR2)	DDR2 System Memory Interface (1.8 V, 533 MTs) Supply Current		1 Channel 2 Channel	1200 2400	mA mA	
I_{SUS_VCCSM} (DDR2)	DDR2 System Memory Interface (1.8 V) Standby Supply Current		1 Channel 2 Channel	~ 5 ~ 5	mA	Number is same for 400 MTs and 533MTs
I_{SMVREF} (DDR2)	DDR2 System Memory Interface Reference Voltage (0.90 V) Supply Current			10	µA/pin	
I_{SUS_SMVREF} (DDR2)	DDR2 System Memory Interface Reference Voltage (0.90 V) Standby Supply Current			10	µA/pin	
I_{TTRC} (DDR2)	DDR2 System Memory Interface Resister Compensation Voltage (1.8 V) Supply Current			32	mA	
I_{SUS_TTRC} (DDR2)	DDR2 System Memory Interface Resister Compensation Voltage (1.8 V) Standby Supply Current			~ 0	µA	
I_{VCCASM}	Memory DLL (400 MTs)		1 Channel 2 Channel	215 290	mA	
I_{VCCASM}	Memory DLL (533 MTs)		1 Channel 2 Channel	280 390	mA	
I_{SUS_VCCASM}	Memory DLL (Standby)		1 Channel 2 Channel	0 0	mA	

NOTE: Standby or Sus in Table 3 and Table 4 refers to system memory in Self Refresh during S3 Cold (STR).

11.3 Signal Groups

The signal description includes the type of buffer used for the particular signal:

AGTL+ Open Drain AGTL+ interface signal. Refer to the AGTL+ I/O Specification for complete details. (VCCP)

Analog Analog signal interface

CMOS CMOS buffers. 1.5 V tolerant

HVCMOS CMOS buffers. 2.5 V tolerant

COD CMOS Open Drain buffers. 2.5 V tolerant

DDR DDR system memory (2.5 V CMOS buffers)

DDR2 DDR2 system memory (1.8 V CMOS buffers)

PCI Express* GFX/Serial DVO PCI Express interface signals. These signals are compatible with PCI Express Base Specification 1.0a Electrical Signal Specifications. The buffers are not 3.3 V tolerant. Differential voltage spec = (|D+ - D-|) * 2 = 1.2 V max. Single-ended maximum = 1.5V. Single-ended minimum = 0V. Please refer to the PCIE specification.

SSTL-2 2.5 V tolerant Stub Series Termination Logic

SSTL-1.8 1.8 V tolerant Stub Series Termination Logic

LVDS Low Voltage Differential Signal interface

Ref Voltage reference signal

Table 11-5. Signal Groups

Signal Group	Signal Type	Signals	Notes
Host Interface Signal Groups			
(a)	AGTL+ Input/Output	HADS#, HBNR#, HBREQ0#,HDBSY#, HDRDY#, HDINV[3:0]#, HA[31:3]#, HADSTB[1:0]#, HD[63:0]#,HDSTBP[3:0]#, HDSTBN[3:0]#, HHIT#, HHITM#, HREQ[4:0]#	
(b)	AGTL+ Common Clock Outputs	HBPRI#, HCPURST#, HDEFER#, HTRDY#, HRS[2:0]#, HDPWR#	
(c)	CMOS Output	HCPUSLP#, THRMTRIP#	CMOS Type Buffer with Vtt
(d)	AGTL+ Asynchronous Input	HLOCK#	
(e)	Analog Host I/F Ref & Comp. Signals	HVREF, HXSWING, HYSWING, HXRCOMP, HXSCOMP, HYRCOMP, HYSCOMP	
Serial DVO or PCI-Express Graphics Interface Signal Groups			
(f)	PCI-E GFX/SDVO Input	**PCI-E GFX Interface:** EXP_RXN[15:0], EXP_RXP[15:0], **SDVO Interface:** SDVO_TVCLKIN#, SDVO_TVCLKIN, SDVOB_INT#, SDVOB_INT, SDVOC_INT#, SDVOC_INT, SDVO_FLDSTALL#, SDVO_FLDSTALL	Please see Signal Description chapter for SDVO & PCI Express GFX Pin Mapping
(g)	PCI-E GFX/SDVO Output	**PCI-E GFX Interface:** EXP_TXN[15:0], EXP_TXP[15:0] **SDVO Interface:** SDVOB_RED#, SDVOB_RED, SDVOB_GREEN#, SDVOB_GREEN, SDVOB_BLUE#, SDVOB_BLUE, SDVOB_CLKN, SDVOB_CLKP, SDVOC_RED#/SDVOB_ALPHA#, SDVOC_RED/SDVOB_ALPHA, SDVOC_GREEN#, SDVOC_GREEN, SDVOC_BLUE#, SDVOC_BLUE, SDVOC_CLKN, SDVOC_CLKP	Please see Signal Description chapter for SDVO & PCI Express GFX Pins Mapping
(h)	Analog PCI-E GFX/SDVO I/F Compensation Signals	EXP_ICOMP0 EXP_COMPI	
DDR Interface Signal Groups			
(i)	SSTL- 2 DDR CMOS I/O	DQ (SA_DQ[63:0], SB_DQ[63:0]) DQS (SA_DQS[7:0], SB_DQS[7:0])	
(j)	SSTL – 2 DDR CMOS Output	DM (SA_DM[7:0], SB_DM[7:0]) MA (SA_MA[13:0], SB_MA[13:0]) BS (SA_BS[1:0], SB_BS[1:0]) RAS# (SA_RAS#, SB_RAS#) CAS# (SA_CAS#, SB_CAS#) WE# (SA_WE#, SB_WE#) SM_CKE[3:0], SM_CS[3:0]#, SM_CK[4:3,1:0], SM_CK[4:3,1:0]#	
(k)	DDR Reference Voltage	SMVREF(1:0)	

Signal Group	Signal Type	Signals	Notes
DDR2 Interface Signal Groups			
(l)	SSTL – 1.8 DDR2 CMOS I/O	DQ (SA_DQ[63:0], SB_DQ[63:0]) DQS (SA_DQS[7:0], SB_DQS[7:0]) DQS# (SA_DQS[7:0]#, SB_DQS[7:0]#)	
(m)	SSTL – 1.8 DDR2 CMOS Output	DM (SA_DM[7:0], SB_DM[7:0]) MA (SA_MA[13:0], SB_MA[13:0]) BS (SA_BS[2:0], SB_BS[2:0]) RAS# (SA_RAS#, SB_RAS#) CAS# (SA_CAS#, SB_CAS#) WE# (SA_WE#, SB_WE#), SM_ODT[3:0], SM_CKE[3:0], SM_CS[3:0]#, SM_CK[4:3,1:0], SM_CK[4:3,1:0]#	
(n)	DDR2 Reference Voltage	SMVREF(1:0)	
LVDS Signal Groups			
(o)	LVDS LVDS Input/Output	LADATAP[2:0], LADATAN[2:0], LACLKP, LACLKN, LBDATAP[2:0], LBDATAN[2:0], LBCLKP, LBCLKN	
	Analog LVDS Miscellaneous	LIBG	Current Mode Reference pin. DC Spec. not required
CRT DAC Signal Groups			
	Analog Current Outputs	RED, RED#, GREEN, GREEN#, BLUE, BLUE#	Please refer to Section 11.4.2
	Analog/Ref DAC Miscellaneous	REFSET	Current Mode Reference pin. DC Spec. not required
	HVCMOS Type	HSYNC, VSYNC	Please refer to the VESA specification for details
TV DAC Signal Groups (these signals are not supported on the Intel 915GME / Intel 910GMLE chipsets)			
	Analog Current Outputs	TVDAC_A, TVDAC_B, TVDAC_C, TV_IRTNA, TV_IRTNB, TV_IRTNC	
	Analog/Ref DAC Miscellaneous	TV_REFSET	Current Mode Reference pin. DC Spec. not required
Clocks, Reset, and Miscellaneous Signal Groups			
(p)	HVCMOS Input	EXT_TS[1:0]#, CFG[20:18], CFG[2:0]	
(q)	Low Voltage Diff.	HCLKP(BCLK/BCLK0), HCLKN(BCLK#/BCLK1),	

Signal Group	Signal Type	Signals	Notes
	Clock Input	DREF_CLKP, DREF_CLKN, DREF_SSCLKP, DREF_SSCLKN, GCLKP, GCLKN	
(r)	HVCMOS Output	BM_BUSY#, LVDD_EN, LBKLT_EN, LBKLT_CTRL	
(s)	HVCMOS I/O	DDCCLK, DDCDATA, LDDC_CLK, LDDC_DATA, SDVOCTRL_CLK, SDVOCTRL_DATA, LCTLB_DATA, LCTLA_CLK	
(t)	AGTL+ Input/Output	CFG[17:3], RSVD	
(u)	MISC	RSTIN#, PWROK	
I/O Buffer Supply Voltages			
(v)	AGTL+ Termination Voltage	VTT (Vccp)	
(w)	SDVO, DMI, PCI Express GFX Voltages	VCC3G, VCCA_3GBG	
(x)	2.5 V DDR Supply Voltage	VCCSM (DDR)	
(y)	1.8V DDR2 Supply Voltage	VCCSM (DDR2)	
(z)	1.5 V DDR/DDR2 Analog Supply	VCCA_SM	
(aa)	GMCH Core	VCC	
(ab)	HV Supply Voltage	VCCHV	
(ac)	TV DAC Supply Voltage	VCCD_TVDAC, VCCDQ_TVDAC	
(ad)	TV DAC Band Gap and Channel Supply	VCCA_TVBG, VCCA_TVDACA,VCCA_TVDACB, VCCA_TVDACC	
(ae)	CRT DAC Supply Voltage	VCCA_CRTDAC, VCC_SYNC	
(af)	PLL Supply Voltages	VCCA_HPLL, VCCA_MPLL, VCCD_HMPLL VCCA_3GPLL, VCCA_DPLLA, VCCA_DPLLB	
(ag)	1.5 V LVDS Digital Supply	VCCD_LVDS	
(ah)	2.5 V LVDS Data/CLK Transmitter Supply	VCCTX_LVDS	
(ai)	2.5 V LVDS Analog Supply	VCCA_LVDS	

11.4 DC Characteristics

11.4.1 General DC Characteristics

Table 11-6. DC Characteristics

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
I/O Buffer Supply Voltage (AC Noise not included)							
VCC	(aa)	1.05 V GMCH Core Supply Voltage	1.0	1.05	1.1	V	
VCC	(aa)	1.5 V GMCH Core Supply Voltage	1.425	1.5	1.575	V	
VTT	(v)	1.05 V Host AGTL+ Termination Voltage	0.9475	1.05	1.1025	V	
VCCSM (DDR)	(x)	DDR I/O Supply Voltage	2.3	2.5	2.7	V	
VCCSM (DDR2)	(y)	DDR2 I/O Supply Voltage	1.7	1.8	1.9	V	
VCCASM (DDR)	(z)	DDR I/O Analog Supply	1.425	1.5	1.575	V	
VCCASM (DDR2)	(z)	DDR2 I/O Analog Supply	1.425	1.5	1.575	V	
VCC3G	(w)	DMI, SDVO, PCI Express GFX Supply Voltage	1.425	1.5	1.575	V	
VCCA_3GBG	(w)	DMI, SDVO, PCI Express GFX Analog Voltage	2.32	2.5	2.625	V	
VCCHV	(ab)	HV CMOS Supply Voltage	2.375	2.5	2.625	V	
VCCD_TVDAC	(ac)	TV DAC Supply Voltage	1.425	1.5	1.575	V	
VCCDQ_TVDAC	(ac)	TV DAC Quiet Supply Voltage	1.425	1.5	1.575	V	
VCCA_TVDACA VCCA_TVDACB VCCA_TVDACC VCCA_TVBG	(ad)	TV DAC Analog & Band Gap Supply Voltage	3.135	3.3	3.465	V	
VCCA_CRTDAC	(ae)	CRT DAC Supply Voltage	2.32	2.5	2.625	V	
VCC_SYNC	(ae)	CRT DAC SYNC Supply Voltage	2.32	2.5	2.625	V	
VCCA_HPLL, VCCA_MPLL, VCCD_HMPLL VCCA_3GPLL, VCCA_DPLLA, VCCA_DPLLB	(af)	Various PLLS Analog Supply Voltages	1.425	1.5	1.575	V	1 -Ripple Noise spec.
VCCD_LVDS	(ag)	Digital LVDS Supply Voltage	1.425	1.5	1.575	V	
VCCTX_LVDS	(ah)	Data/Clock Transmitter LVDS Supply Voltage	2.375	2.5	2.625	V	
VCCA_LVDS	(ai)	Analog LVDS Supply Voltage	2.375	2.5	2.625	V	
Reference Voltages							
HVREF	(e)	Host Address and Data Reference Voltage	2/3 x VTT – 2%	2/3 x VTT	2/3 x VTT + 2%	V	
HXSWING HYSWING	(e)	Host Compensation Reference Voltage	0.3125 x VTT – 2%	0.3125x VTT	0.3125x VTT + 2%	V	
SMVREF (DDR)	(k)	DDR Reference Voltage	0.5VCCSM - 0.05	0.50 x VCCSM	0.5VCCSM + 0.05	V	

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
SMVREF (DDR2)	(n)	DDR2 Reference Voltage	0.49 x VCCSM	0.50 x VCCSM	0.51 x VCCSM	V	
Host Interface							
V_{IL_H}	(a,d,t)	Host AGTL+ Input Low Voltage	-0.10	0	(2/3 x VTT) – 0.1	V	
V_{IH_H}	(a,d,t)	Host AGTL+ Input High Voltage	(2/3 x VTT) + 0.1	VTT (1.05)	VTT + 0.1	V	
V_{OL_H}	(a,b,t)	Host AGTL+ Output Low Voltage			(0.3125 x VTT) + 0.1	V	
V_{OH_H}	(a,b,t)	Host AGTL+ Output High Voltage	VTT-0.1		VTT	V	
I_{OL_H}	(a,b,t)	Host AGTL+ Output Low Current			VTT_{max} / (1-0.3125)Rtt_{min}	mA	Rtt_{min}=50 ohm
I_{LEAK_H}	(a,d,t)	Host AGTL+ Input Leakage Current			20	uA	V_{OL}<Vpad< Vtt
C_{PAD}	(a,d,t)	Host AGTL+ Input Capacitance	2		3.5	pF	
V_{OL_H}	(c)	CMOS Output Low Voltage			0.1 VTT	V	I_{OL} = 1 mA
V_{OH_H}	(c)	CMOS Output High Voltage	0.9VTT		VTT	V	I_{OH} = 1 mA
DDR Interface							
$V_{IL(DC)}$ (DDR)	(i)	DDR Input Low Voltage			SMVREF – 0.15	V	
$V_{IH(DC)}$ (DDR)	(i)	DDR Input High Voltage	SMVREF + 0.15			V	
$V_{IL(AC)}$ (DDR)	(i)	DDR Input Low Voltage			SMVREF – 0.31	V	
$V_{IH(AC)}$ (DDR)	(i)	DDR Input High Voltage	SMVREF + 0.31			V	
V_{OL} (DDR)	(i, j)	DDR Output Low Voltage			0.4	V	2
V_{OH} (DDR)	(i, j)	DDR Output High Voltage	2.1			V	2
I_{Leak} (DDR)	(i)	Input Leakage Current			±10	µA	
$C_{I/O}$ (DDR)	(i, j)	DDR Input/Output Pin Capacitance	3.0		6.0	pF	
DDR2 Interface							
$V_{IL(DC)}$ (DDR2)	(l)	DDR2 Input Low Voltage			SMVREF – 0.125	V	
$V_{IH(DC)}$ (DDR2)	(l)	DDR2 Input High Voltage	SMVREF + 0.125			V	
$V_{IL(AC)}$ (DDR2)	(l)	DDR2 Input Low Voltage			SMVREF – 0.250	V	
$V_{IH(AC)}$ (DDR2)	(l)	DDR2 Input High Voltage	SMVREF + 0.250			V	
V_{OL} (DDR2)	(l, m)	DDR2 Output Low Voltage			0.3	V	2
V_{OH} (DDR2)	(l, m)	DDR2 Output High Voltage	1.5			V	2
I_{Leak} (DDR2)	(l)	Input Leakage Current			±10	uA	

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
$C_{I/O}$ (DDR2)	(l, m)	DDR2 Input/Output Pin Capacitance	3.0		6.0	pF	
1.5 V PCI Express Interface 1.0a (includes PCI Express GFX and SDVO)							
$V_{TX-DIFF\ P-P}$	(f, g)	Differential Peak to Peak Output Voltage	0.400		0.6	V	3, 4
V_{TX_CM-ACp}	(f, g)	AC Peak Common Mode Output Voltage			20	mV	3
$Z_{TX-DIFF-DC}$	(f, g)	DC Differential TX Impedance	80	100	120	Ω	
$V_{RX-DIFF\ p-p}$	(f, g)	Differential Input Peak to Peak Voltage	0.175		1.2	V	3, 4
V_{RX_CM-ACp}	(f, g)	AC peak Common Mode Input Voltage			150	mV	
Clocks, Reset, and Miscellaneous Signals							
V_{IL}	(p)	Input Low Voltage			0.8	V	
V_{IH}	(p)	Input High Voltage	2.0			V	
I_{LEAK}	(p)	Input Leakage Current			±10	µA	
C_{IN}	(p)	Input Capacitance	3.0		6.0	pF	
V_{IL}	(q)	Input Low Voltage		0		V	
V_{IH}	(q)	Input High Voltage	0.660	0.710	0.850	V	
V_{CROSS}	(q)	Crossing Voltage	0.45x(V_{IH} - V_{IL})	0.5x(V_{IH} - V_{IL})	0.55x(V_{IH} - V_{IL})	V	
C_{IN}	(q)	Input Capacitance	0.5		1.5	pF	
V_{OL}	(r, s)	Output Low Voltage (CMOS Outputs)			0.4	V	
V_{OH}	(r, s)	Output High Voltage (CMOS Outputs)	2.1			V	
I_{OL}	(r, s)	Output Low Current (CMOS Outputs)			1	mA	@V_{OL_HI} max
I_{OH}	(r, s)	Output High Current (CMOS Outputs)	-1			mA	@V_{OH_HI} min
V_{IL}	(s)	Input Low Voltage (DC)			(Vcchv/2) - 0.2	V	
V_{IH}	(s)	Input High Voltage (DC)	(vcchv/2) + 0.2			V	
I_{LEAK}	(s)	Crossing Voltage			±10	uA	
C_{IN}	(s)	Input Capacitance	3.0		6.0	pF	
V_{IL}	(u)	Input Low Voltage			0.8	V	
V_{IH}	(u)	Input High Voltage	2.0			V	
I_{LEAK}	(u)	Input Leakage Current			±100	µA	0<Vin<VCC3_3
C_{IN}	(u)	Input Capacitance	4.690		5.370	pF	
LVDS Interface: Functional Operating Range (VCC=2.5 V±5%)							
V_{OD}	(o)	Differential Output Voltage	250	350	450	mV	

Symbol	Signal Group	Parameter	Min	Nom	Max	Unit	Notes
ΔV_{OD}	(o)	Change in V_{OD} between Complementary Output States			50	mV	
V_{OS}	(o)	Offset Voltage	1.125	1.25	1.375	V	
ΔV_{OS}	(o)	Change in V_{OS} between Complementary Output States			50	mV	
I_{Os}	(o)	Output Short Circuit Current		-3.5	-10	mA	
I_{OZ}	(o)	Output TRI-STATE Current		±1	±10	µA	

NOTES:

1. Following are the noise rejection specifications for PLL supplies.

VCCA_HPLL	34 dB(A) attenuation of power supply noise in 1 MHz(f1) to 66 MHz(f2) range, <0.2 dB gain in pass band and peak to peak noise should be limited to < 120 mV
VCCA_MPLL	34 dB(A) attenuation of power supply noise in 1 MHz(f1) to 66MHz(f2) range, <0.2 dB gain in pass band and peak to peak noise should be limited to < 120 mV
VCCD_HMPLL	peak to peak noise should be limited to < 120 mV
VCCA_3GPLL	< 0 dB(A) in 0 to 1MHz, 20 dB(A) attenuation of power supply noise in 1 MHz(f1) to 1.25 GHz(f2) range, <0.2 dB gain in pass band and peak to peak noise should be limited to < 40 mV
VCCA_DPLLA	20 dB(A) attenuation of power supply noise in 10 kHz(f1) to 2.5 MHz(f2) range, <0.2 dB gain in pass band and peak to peak noise should be limited to < 100 mV
VCCA_DPLLB	20 dB(A) attenuation of power supply noise in 10 kHz(f1) to 2.5 MHz(f2) range, <0.2 dB gain in pass band and peak to peak noise should be limited to < 100 mV
VccASM(DDR2)	30 dB(A) attenuation of power supply noise in 50 MHz (f1) to 266 MHz (f2), < 0.2 dB gain in pass band and peak to peak noise should be limited to < 120 mv
Vcc3G	< 0 dB(A) in 0 to 1.5 MHz, 20 dB(A) attenuation of power supply noise in 1.5 MHz(f1) to 1.25 GHz(f2) range, <0.2 dB gain in pass band and peak to peak noise should be limited to < 40 mV

2. Determined with 2x GMCH DDR/DDR2 buffer strength settings into a 50 Ω to 0.5xVCCSM (DDR/DDR2) test load.
3. Specified at the measurement point into a timing and voltage compliance test load as shown in Transmitter compliance eye diagram of PCI Express specification and measured over any 250 consecutive TX UI's. Specified at the measurement point and measured over any 250 consecutive ULS. The test load shown in receiver compliance eye diagram of PCI Express specification. Should be used as the RX device when taking measurements.
4. Low voltage PCI Express (PCI Express Graphics/SDVO) interface.

11.4.2 CRT DAC DC Characteristics

Table 11-7. CRT DAC DC Characteristics: Functional Operating Range (VCCADAC = 2.5 V ±5%)

Parameter	Min	Typical	Max	Units	Notes
DAC Resolution		8		Bits	(1)
Max Luminance (full-scale)	0.665	0.700	0.770	V	(1, 2, 4) white video level voltage
Min Luminance		0.000		V	(1, 3, 4) black video level voltage
LSB Current		73.2		µA	(4, 5)
Integral Linearity (INL)	-1.0		+1.0	LSB	(1, 6)
Differential Linearity (DNL)	-1.0		+1.0	LSB	(1, 6)
Video channel-channel voltage amplitude mismatch			6	%	(7)
Monotonicity	Guaranteed				

NOTES:
1. Measured at each R, G, B termination according to the VESA Test Procedure – Evaluation of Analog Display Graphics Subsystems Proposal (Version 1, Draft 4, December 1, 2000).
2. Max steady-state amplitude
3. Min steady-state amplitude
4. Defined for a double 75-Ω termination.
5. Set by external reference resistor value.
6. INL and DNL measured and calculated according to VESA video signal standards.
7. Max full-scale voltage difference among R,G,B outputs (percentage of steady-state full-scale voltage).

11.4.3 TV DAC DC Characteristics (not supported on the Intel 915GME/Intel 910GMLE chipsets)

Table 11-8. TV DAC DC Characteristics: Functional Operating Range (VCCATVDAC[A,B,C] = 3.3 V ±5%)

Parameter	Min	Typical	Max	Units	Notes
DAC Resolution	10			Bits	Measured at low-frequency
ENOB (Effective Number of Bits)	7.5			Bits	@ NTSC/PAL Video BW
Integral Linearity (INL)	-0.5		+0.5	LSB	Note: 1
Differential Linearity (DNL)	-0.5		+0.5	LSB	Note: 1
SNR	48			dB	RMS @ NTSC/PAL Video BW
Video channel-channel voltage amplitude mismatch	-3		+3	%	Note: 2
Monotonicity	Guaranteed				

NOTES:
1. INL and DNL measured and calculated based on the method given in VESA video signal standards.
2. Max full-scale voltage difference among the outputs (percentage of steady-state full-scale voltage).

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12 GMCH Strap Pins

12.1 Mobile Intel 915 and 910 Express Chipset Family Strapping Configuration

Only HW straps CFG{2:0} and CFG [6:5] are used for Mobile Intel 915GMS Express Chipset.

Table 12-1. Mobile Intel 915 Express Chipset Family Strapping Signals and Configuration

Pin Name	Strap Description	Configuration	Notes
CFG[2:0]	FSB Frequency Select	000 = Reserved 001 = FSB533 010 = Reserved 011 = Reserved 100 = Reserved 101 = FSB400 110 = Reserved 111 = Reserved	
CFG[4:3]	Reserved		
CFG5	DMI x2 Select	0 = DMI X2 **1 = DMI X4** (Default)	
CFG6	DDR vs DDR2 select	0 = DDR2 **1 = DDR** (Default)	
CFG7	CPU Strap	0 = Reserved **1 = Intel Pentium M Processor with 2 MBL2 Cache** (Default)	
CFG8	Reserved		
CFG9	PCI Express Graphics Lane Reversal	0 = Reserve Lanes (15->0, 14->1 etc) **1 = Normal Operation** (Default)	
CFG[11:10]	Reserved		
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled **11 = Normal Operation** (Default)	
CFG[15:14]	Reserved		
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled	

Pin Name	Strap Description	Configuration	Notes
		1 = Dynamic ODT Enabled (Default)	
CFG17	Reserved		
CFG18	GMCH core VCC Select	**0 = 1.05 V (Default)** 1 = 1.5 V	
CFG19	CPU VTT Select	**0 = 1.05 V (Default)** 1 = 1.2 V (Reserved)	
CFG20	Reserved		
SDVOCRTL_ DATA	SDVO Present	**0 = No SDVO device present (Default)** 1 = SDVO device present	

NOTES: All strap signals are sampled with respect to the leading edge of the Mobile Intel 915/910 Express Chipset Family PWROK In signal.

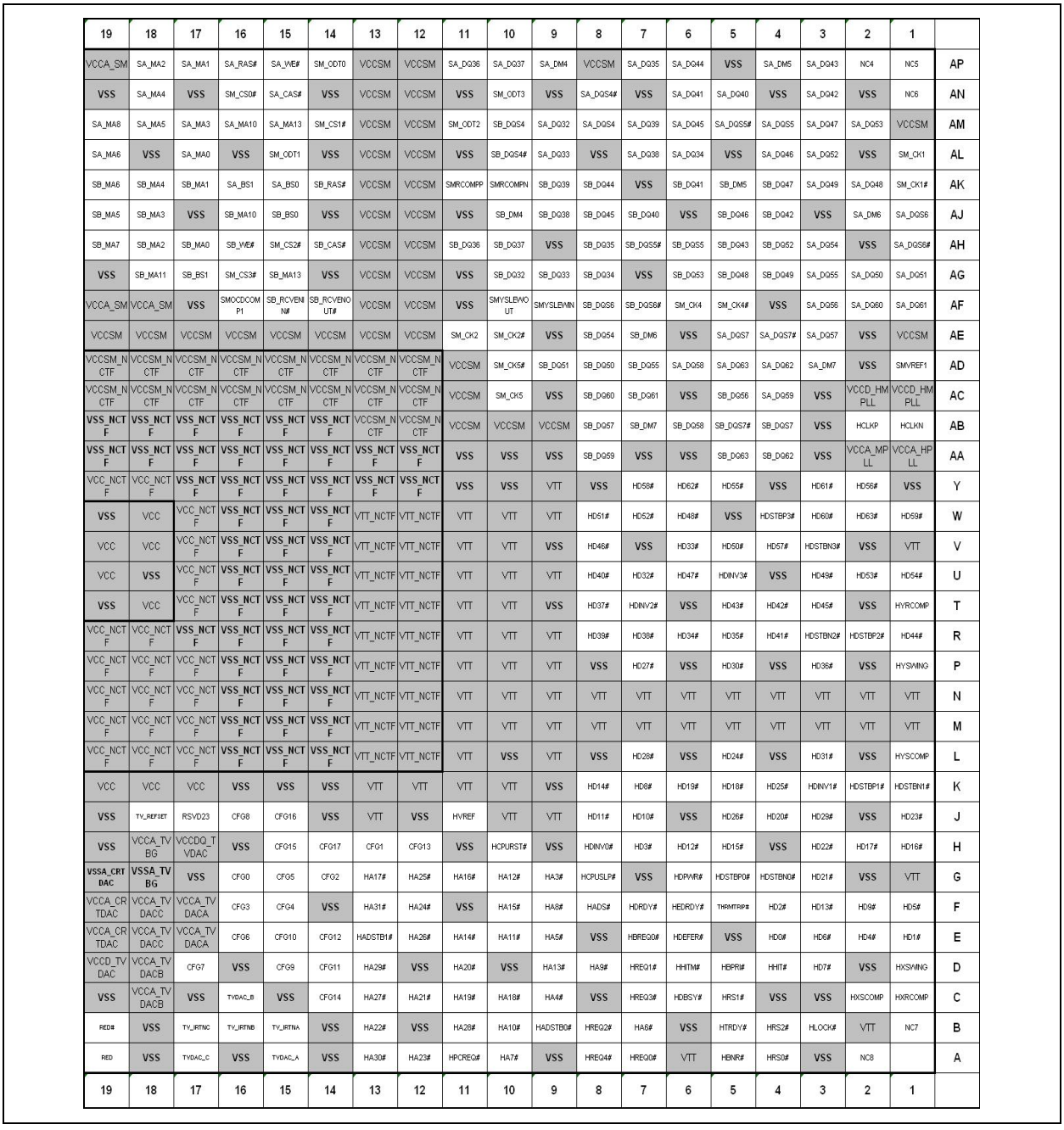
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13 Ballout and Package Information

Figure 13-1. Intel 915GM, 915GME, 915PM, 910GML, 910GMLE Express Chipset GMCH Ballout Diagram (Top Left)

	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20
AP	NC1	NC3	SA_DM1	SA_DQS1#	SA_DQS1	SA_DQ10	SA_DQ17	VSS	VCCSM	SA_DQ19	SA_DQ24	VCCSM	VCCSM	SA_DM3	SA_DQS3	SA_DQ31	SM_CKE0	SA_MA7
AN	NC2	VSS	SA_DQ9	VSS	SM_CK0#	VSS	SA_DQ16	SA_DQS2#	SA_DQS2	SA_DQ18	VSS	VCCSM	VCCSM	VSS	SA_DQS3#	SA_DQ30	VSS	SA_MA11
AM	VCCSM	SA_DQ8	SA_DQ13	SA_DQ12	SM_CK0	SA_DQ15	SA_DQ11	SA_DQ21	VSS	SA_DQ22	SA_DQ25	VCCSM	VCCSM	SA_DQ29	SA_DQ26	SA_DQ27	SM_CKE1	SA_MA12
AL	SA_DQ3	VSS	SA_DQ2	SA_DQ7	VSS	SA_DQ14	VSS	SA_DQ20	SA_DM2	SA_DQ23	VSS	VCCSM	VCCSM	VSS	SA_DQ28	VSS	SA_BS2	SA_MA9
AK	SA_DQ6	SA_DQS0	SA_DQS0#	SB_DM1	SB_DQS1#	SB_DQS1	SB_DQ10	SB_DQ16	SB_DQ20	SB_DQS2#	SB_DM2	VCCSM	VCCSM	SB_DM3	SB_DQS3	SB_DQ27	SM_CKE3	VSS
AJ	SA_DM0	VSS	SA_DQ5	SM_CK3	SM_CK3#	VSS	SB_DQ15	SB_DQ17	VSS	SB_DQS2	VSS	VCCSM	VCCSM	VSS	SB_DQS3#	SB_DQ26	SB_DQ31	SB_MA8
AH	VCCSM	SA_DQ4	SA_DQ1	VSS	SB_DQ8	SB_DQ9	SB_DQ14	SB_DQ21	SB_DQ18	SB_DQ19	SB_DQ22	VCCSM	VCCSM	SB_DQ28	SB_DQ29	VSS	SM_CKE2	SB_MA9
AG	VSS	SB_DQ3	SA_DQ0	SB_DQ12	SB_DQ13	SB_DQ2	VSS	SB_DQ11	VSS	SB_DQ23	VSS	VCCSM	VCCSM	VSS	SB_DQ25	SB_DQ30	SB_BS2	SB_MA12
AF	SMVREF0	VSS	SB_DQS0#	SB_DQS0	VSS	SB_DM0	SB_DQ6	SB_DQ7	SA_RCVENIN#	SA_RCVENOUT#	VSS	VCCSM	VCCSM	SB_DQ24	VSS	SMOCDCOMP0	VSS	VCCA_SM
AE	VCC3G	VSS	VSS	SB_DQ4	SB_DQ5	SB_DQ1	SB_DQ0	VSS	RSTIN#	SMXSLEWOUT	SMXSLEWIN	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM
AD	DMI_TXN3	VSS	DMI_RXN3	VSS	VSS	VSS	VSS	PWROK	VSS	VCCSM	VCCSM	VCCSM_NCTF	VCCSM_NCTF	VCCSM_NCTF	VCCSM_NCTF	VCCSM_NCTF	VCCSM_NCTF	VCCSM_NCTF
AC	DMI_TXP3	VSS	DMI_RXP3	VSS	DMI_TXN2	VSS	DMI_RXN2	VSS	GCLKP	VSS	VCCSM	VCCSM_NCTF	VCCSM_NCTF	VCCSM_NCTF	VCCSM_NCTF	VCCSM_NCTF	VCCSM_NCTF	VCCSM_NCTF
AB	DMI_TXN1	VSS	DMI_RXN1	VSS	DMI_TXP2	VSS	DMI_RXP2	VSS	GCLKN	VSS	VSS	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF
AA	DMI_TXP1	VSS	DMI_RXP1	VSS	DMI_TXN0	VSS	DMI_RXN0	VSS	VSS	VSS	VSS	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF
Y	VSS	EXP_TXN15	VSS	EXP_RXN15	DMI_TXP0	VSS	DMI_RXP0	VSS	VCCA_3GPLL	VCCA_3GPLL	VCCA_3GPLL	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VCC_NCTF
W	VCC3G	EXP_TXP15	VSS	EXP_RXP15	VSS	EXP_TXN14	VSS	EXP_RXN14	VSS	VSS	VSS	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC
V	VSS	EXP_TXN13	VSS	EXP_RXN13	VSS	EXP_TXP14	VSS	EXP_RXP14	VSS	VCC	VCC	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VSS
U	VCC3G	EXP_TXP13	VSS	EXP_RXP13	VSS	EXP_TXN12	VSS	EXP_RXN12	VSS	VCC	VCC	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC
T	VSS	EXP_TXN11	VSS	EXP_RXN11	VSS	EXP_TXP12	VSS	EXP_RXP12	VCC	VCC	VCC	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC
R	VCC3G	EXP_TXP11	VSS	EXP_RXP11	VSS	EXP_TXN10	VSS	EXP_RXN10	VCC	VCC	VCC	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VSS_NCTF	VCC_NCTF
P	VSS	EXP_TXN9	VSS	EXP_RXN9	VSS	EXP_TXP10	VSS	EXP_RXP10	VSS	VCC	VCC	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF
N	VCC3G	EXP_TXP9	VSS	EXP_RXP9	VSS	EXP_TXN8	VSS	EXP_RXN8	VCC	VCC	VCC	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF
M	VSS	EXP_TXN7	VSS	EXP_RXN7	VSS	EXP_TXP8	VSS	EXP_RXP8	VCC	VCC	VCC	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF
L	VCC3G	EXP_TXP7	VSS	EXP_RXP7	VSS	EXP_TXN6	VSS	EXP_RXN6	VSS	VCC	VCC	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF	VCC_NCTF
K	VSS	EXP_TXN5	VSS	EXP_RXN5	VSS	EXP_TXP6	VSS	EXP_RXP6	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC	VCC
J	VCC3G	EXP_TXP5	VSS	EXP_RXP5	VSS	EXP_TXN4	VSS	EXP_RXN4	VCC	VCC	VCC	VSS	VCC	VSS	BM_BUSY#	VSS	EXT_TS0#	REFSET
H	VSS	EXP_TXN3	VSS	EXP_RXN3	VSS	EXP_TXP4	VSS	EXP_RXP4	VSS	VCC	VCC	VCC	SDVOCTRL_CLK	SDVOCTRL_DATA	VSS	EXT_TS1#	VSYNC	VCC_SYNC
G	VSSA_3GBG	EXP_TXP3	VSS	EXP_RXP3	VSS	EXP_TXN2	VSS	EXP_RXN2	VSS	VCC	VSS	VSS	RSVD21	RSVD22	CFG19	CFG18	HSYNC	VSS
F	VCCA_3GBG	EXP_TXN1	VSS	EXP_RXN1	VSS	EXP_TXP2	VSS	EXP_RXP2	VSS	LVREFH	LVREFL	LVDD_EN	LBKLT_EN	VSS	LDDC_CLK	LDDC_DATA	VSS	VSS
E	VSS	EXP_TXP1	VSS	EXP_RXP1	VSS	EXP_TXN0	VSS	EXP_RXN0	VSS	VSS	VSS	VSS	LBKLT_CRTL	DDCCLK	DDCDATA	VSS	BLUE	VSS
D	DREF_SSCLKP	EXP_COMPI	VSS	EXP_ICOMPO	VSS	EXP_TXP0	VSS	EXP_RXP0	VSS	LBDATAN1	LBDATAP1	RSVD26	RSVD27	VSS	CFG20	VSS	BLUE#	VSS
C	DREF_SSCLKN	VSS	VCCA_DPLLB	VSS	LIBG	VSS	LVBG	VSS	LBDATAN0	LBDATAP0	LBDATAN2	LBDATAP2	LBCLKN	LBCLKP	LCTLA_CLK	LCTLB_DATA	VSS	GREEN
B	NC9	VSSALVDS	VSS	LADATAN0	LADATAN1	LADATAN2	LADATAP2	LACLKN	LACLKP	VCCTX_LVDS	VSS	VCCD_LVDS	VCCD_LVDS	VSS	VCCA_DPLLA	VCCHV	VCCHV	GREEN#
A	NC11	NC10	VCCA_LVDS	LADATAP0	LADATAP1	VSS	RSVD24	RSVD25	VSS	VCCTX_LVDS	VCCTX_LVDS	VSS	VCCD_LVDS	DREF_CLKN	DREF_CLKP	VSS	VCCHV	VSS
	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20

Figure 13-2. Intel 915GM, 915GME, 915PM, 910GML, 910GMLE Express Chipset GMCH Ballout Diagram (Top Right)



19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
VCCA_SM	SA_MA2	SA_MA1	SA_RAS#	SA_WE#	SM_ODT0	VCCSM	VCCSM	SA_DQ36	SA_DQ37	SA_DM4	VCCSM	SA_DQ35	SA_DQ44	VSS	SA_DM5	SA_DQ43	NC4	NC5	AP
VSS	SA_MA4	VSS	SM_CS0#	SA_CAS#	VSS	VCCSM	VCCSM	VSS	SM_ODT3	VSS	SA_DQS4#	VSS	SA_DQ41	SA_DQ40	VSS	SA_DQ42	VSS	NC6	AN
SA_MA8	SA_MA5	SA_MA3	SA_MA10	SA_MA13	SM_CS1#	VCCSM	VCCSM	SM_ODT2	SB_DQS4	SA_DQ32	SA_DQS4	SA_DQ39	SA_DQ45	SA_DQS5#	SA_DQS5	SA_DQ47	SA_DQ53	VCCSM	AM
SA_MA6	VSS	SA_MA0	VSS	SM_ODT1	VSS	VCCSM	VCCSM	VSS	SB_DQS4#	SA_DQ33	VSS	SA_DQ38	SA_DQ34	VSS	SA_DQ46	SA_DQ52	VSS	SM_CK1	AL
SB_MA6	SB_MA4	SB_MA1	SA_BS1	SA_BS0	SB_RAS#	VCCSM	VCCSM	SMRCOMPP	SMRCOMPN	SB_DQ39	SB_DQ44	VSS	SB_DQ41	SB_DM5	SB_DQ47	SA_DQ49	SA_DQ48	SM_CK1#	AK
SB_MA5	SB_MA3	VSS	SB_MA10	SB_BS0	VSS	VCCSM	VCCSM	VSS	SB_DM4	SB_DQ38	SB_DQ45	SB_DQ40	VSS	SB_DQ46	SB_DQ42	VSS	SA_DM6	SA_DQS6	AJ
SB_MA7	SB_MA2	SB_MA0	SB_WE#	SM_CS2#	SB_CAS#	VCCSM	VCCSM	SB_DQ36	SB_DQ37	VSS	SB_DQ35	SB_DQS5#	SB_DQS5	SB_DQ43	SB_DQ52	SA_DQ54	VSS	SA_DQS6#	AH
VSS	SB_MA11	SB_BS1	SM_CS3#	SB_MA13	VSS	VCCSM	VCCSM	VSS	SB_DQ32	SB_DQ33	SB_DQ34	VSS	SB_DQ53	SB_DQ48	SB_DQ49	SA_DQ55	SA_DQ50	SA_DQ51	AG
VCCA_SM	VCCA_SM	VSS	SMOCDCOMP1	SB_RCVENIN#	SB_RCVENOUT#	VCCSM	VCCSM	VSS	SMYSLEWOUT	SMYSLEWIN	SB_DQS6	SB_DQS6#	SM_CK4	SM_CK4#	VSS	SA_DQ56	SA_DQ60	SA_DQ61	AF
VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	VCCSM	SM_CK2	SM_CK2#	VSS	SB_DQ54	SB_DM6	VSS	SA_DQS7	SA_DQS7#	SA_DQ57	VSS	VCCSM	AE
VCCSM_NCTF	VCCSM_NCTF	VCCSM_NCTF	VCCSM_NCTF	VCCSM_NCTF	VCCSM_NCTF	VCCSM_NCTF	VCCSM_NCTF	VCCSM	SM_CK5#	SB_DQ51	SB_DQ50	SB_DQ55	SA_DQ58	SA_DQ63	SA_DQ62	SA_DM7	VSS	SMVREF1	AD
VCCSM_NCTF	VCCSM_NCTF	VCCSM_NCTF	VCCSM_NCTF	VCCSM_NCTF	VCCSM_NCTF	VCCSM_NCTF	VCCSM_NCTF	VCCSM	SM_CK5	VSS	SB_DQ60	SB_DQ61	VSS	SB_DQ56	SA_DQ59	VSS	VCCD_HMPLL	VCCD_HMPLL	AC
VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VCCSM_NCTF	VCCSM_NCTF	VCCSM	VCCSM	VCCSM	SB_DQ57	SB_DM7	SB_DQ58	SB_DQS7#	SB_DQS7	VSS	HCLKP	HCLKN	AB
VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS	VSS	VSS	SB_DQ59	VSS	VSS	SB_DQ63	SB_DQ62	VSS	VCCA_MPLL	VCCA_HPLL	AA
VCC_NCTF	VCC_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS	VSS	VTT	VSS	HD58#	HD62#	HD55#	VSS	HD61#	HD56#	VSS	Y
VSS	VCC	VCC_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VTT_NCTF	VTT_NCTF	VTT	VTT	VTT	HD51#	HD52#	HD48#	VSS	HDSTBP3#	HD60#	HD63#	HD59#	W
VCC	VCC	VCC_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VTT_NCTF	VTT_NCTF	VTT	VTT	VSS	HD46#	VSS	HD33#	HD50#	HD57#	HDSTBN3#	VSS	VTT	V
VCC	VSS	VCC_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VTT_NCTF	VTT_NCTF	VTT	VTT	VTT	HD40#	HD32#	HD47#	HDINV3#	VSS	HD49#	HD53#	HD54#	U
VSS	VCC	VCC_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VTT_NCTF	VTT_NCTF	VTT	VTT	VSS	HD37#	HDINV2#	VSS	HD43#	HD42#	HD45#	VSS	HYRCOMP	T
VCC_NCTF	VCC_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VTT_NCTF	VTT_NCTF	VTT	VTT	VTT	HD39#	HD38#	HD34#	HD35#	HD41#	HDSTBN2#	HDSTBP2#	HD44#	R
VCC_NCTF	VCC_NCTF	VCC_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VTT_NCTF	VTT_NCTF	VTT	VTT	VTT	VSS	HD27#	VSS	HD30#	VSS	HD36#	VSS	HYSWING	P
VCC_NCTF	VCC_NCTF	VCC_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VTT_NCTF	VTT_NCTF	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	N
VCC_NCTF	VCC_NCTF	VCC_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VTT_NCTF	VTT_NCTF	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	M
VCC_NCTF	VCC_NCTF	VCC_NCTF	VSS_NCTF	VSS_NCTF	VSS_NCTF	VTT_NCTF	VTT_NCTF	VTT	VSS	VTT	VSS	HD28#	VSS	HD24#	VSS	HD31#	VSS	HYSCOMP	L
VCC	VCC	VCC	VSS	VSS	VSS	VTT	VTT	VTT	VTT	VSS	HD14#	HD8#	HD19#	HD18#	HD25#	HDINV1#	HDSTBP1#	HDSTBN1#	K
VSS	TV_REFSET	RSVD23	CFG8	CFG16	VSS	VTT	VSS	HVREF	VTT	VTT	HD11#	HD10#	VSS	HD26#	HD20#	HD29#	VSS	HD23#	J
VSS	VCCA_TVBG	VCCDQ_TVDAC	VSS	CFG15	CFG17	CFG1	CFG13	VSS	HCPURST#	VSS	HDINV0#	HD9#	HD12#	HD15#	VSS	HD22#	HD17#	HD16#	H
VSSA_CRTDAC	VSSA_TVBG	VSS	CFG0	CFG5	CFG2	HA17#	HA25#	HA16#	HA12#	HA3#	HCPUSLP#	VSS	HDPWR#	HDSTBP0#	HDSTBN0#	HD21#	VSS	VTT	G
VCCA_CRTDAC	VCCA_TVDACC	VCCA_TVDACA	CFG3	CFG4	VSS	HA31#	HA24#	VSS	HA15#	HA8#	HADS#	HDRDY#	HEDRDY#	THRMTRIP#	HD2#	HD13#	HD9#	HD5#	F
VCCA_CRTDAC	VCCA_TVDACC	VCCA_TVDACA	CFG6	CFG10	CFG12	HADSTB1#	HA26#	HA14#	HA11#	HA5#	VSS	HBREQ0#	HDEFER#	VSS	HD0#	HD6#	HD4#	HD1#	E
VCCD_TVDAC	VCCA_TVDACB	CFG7	VSS	CFG9	CFG11	HA29#	VSS	HA20#	VSS	HA13#	HA9#	HREQ1#	HHITM#	HBPRI#	HHIT#	HD7#	VSS	HXSWING	D
VSS	VCCA_TVDACB	VSS	TVDAC_B	VSS	CFG14	HA27#	HA21#	HA19#	HA18#	HA4#	VSS	HREQ3#	HDBSY#	HRS1#	VSS	VSS	HXSCOMP	HXRCOMP	C
RED#	VSS	TV_IRTNC	TV_IRTNB	TV_IRTNA	VSS	HA22#	VSS	HA28#	HA10#	HADSTB0#	HREQ2#	HA6#	VSS	HTRDY#	HRS2#	HLOCK#	VTT	NC7	B
RED	VSS	TVDAC_C	VSS	TVDAC_A	VSS	HA30#	HA23#	HPCREQ#	HA7#	VSS	HREQ4#	HREQ0#	VTT	HBNR#	HRS0#	VSS	NC8		A
19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

13.1 Intel 915GM, 915GME, 915PM, 910GML and 910GMLE Express Chipset GMCH Ballout List

Some signals may be RESERVED depending on which chipset configuration used. Please refer to the signal description chapter for more details for which signals are supported for each chipset.

Table 13-1. PLL Signal Group

Ball	Signal
AB29	GCLKN
AC29	GCLKP
AB1	HCLKN
AB2	HCLKP
A24	DREF_CLKN
A23	DREF_CLKP
C37	DREF_SSCLKN
D37	DREF_SSCLKP

Table 13-2.Host Address Signal Group

Ball	Signal
G9	HA3#
C9	HA4#
E9	HA5#
B7	HA6#
A10	HA7#
F9	HA8#
D8	HA9#
B10	HA10#
E10	HA11#
G10	HA12#
D9	HA13#
E11	HA14#

Ball	Signal
F10	HA15#
G11	HA16#
B9	HADSTB0#
A7	HREQ0#
D7	HREQ1#
B8	HREQ2#
C7	HREQ3#
A8	HREQ4#
G13	HA17#
C10	HA18#
C11	HA19#
D11	HA20#

Ball	Signal
C12	HA21#
B13	HA22#
A12	HA23#
F12	HA24#
G12	HA25#
E12	HA26#
C13	HA27#
B11	HA28#
D13	HA29#
A13	HA30#
F13	HA31#
E13	HADSTB1#

Table 13-3. Host Control Signal Group

Ball	Signal
F8	HADS#
A5	HBNR#
D5	HBPRI#
B5	HTRDY#
F6	RSVD32
F7	HDRDY#

Ball	Signal
C6	HDBSY#
E6	HDEFER#
B3	HLOCK#
E7	HBREQ0#
A11	RSVD33
A4	HRS0#

Ball	Signal
C5	HRS1#
B4	HRS2#
D4	HHIT#
D6	HHITM#
G6	HDPWR#
G8	HSLPCPU#

Table 13-4. Host Data Signal Group

Ball	Signal
E4	HD0#
E1	HD1#
F4	HD2#
H7	HD3#
E2	HD4#
F1	HD5#
E3	HD6#
D3	HD7#
K7	HD8#
F2	HD9#
J7	HD10#
J8	HD11#
H6	HD12#
F3	HD13#
K8	HD14#
H5	HD15#
H8	HDINV0#
G4	HDSTBN0#
G5	HDSTBP0#
H1	HD16#
H2	HD17#
K5	HD18#
K6	HD19#
J4	HD20#
G3	HD21#
H3	HD22#

Ball	Signal
J1	HD23#
L5	HD24#
K4	HD25#
J5	HD26#
P7	HD27#
L7	HD28#
J3	HD29#
P5	HD30#
L3	HD31#
K3	HDINV1#
K1	HDSTBN1#
K2	HDSTBP1#
U7	HD32#
V6	HD33#
R6	HD34#
R5	HD35#
P3	HD36#
T8	HD37#
R7	HD38#
R8	HD39#
U8	HD40#
R4	HD41#
T4	HD42#
T5	HD43#
R1	HD44#
T3	HD45#

Ball	Signal
V8	HD46#
U6	HD47#
T7	HDINV2#
R3	HDSTBN2#
R2	HDSTBP2#
W6	HD48#
U3	HD49#
V5	HD50#
W8	HD51#
W7	HD52#
U2	HD53#
U1	HD54#
Y5	HD55#
Y2	HD56#
V4	HD57#
Y7	HD58#
W1	HD59#
W3	HD60#
Y3	HD61#
Y6	HD62#
W2	HD63#
U5	HDINV3#
V3	HDSTBN3#
W4	HDSTBP3#

Table 13-5. DDR / DDR2 SDRAM Common Signal Group Ball List

Ball	Signal
AM33	SM_CK0
AN33	SM_CK0#
AL1	SM_CK1
AK1	SM_CK1#
AE11	RSVD28
AE10	RSVD29
AJ34	SM_CK3
AJ33	SM_CK3#

Ball	Signal
AF6	SM_CK4
AF5	SM_CK4#
AC10	RSVD30
AD10	RSVD31
AP21	SM_CKE0
AM21	SM_CKE1
AH21	SM_CKE2
AK21	SM_CKE3

Ball	Signal
AN16	SM_CS0#
AM14	SM_CS1#
AH15	SM_CS2#
AG16	SM_CS3#
AP14	SM_ODT0
AL15	SM_ODT1
AM11	SM_ODT2
AN10	SM_ODT3

Table 13-6. DDR / DDR2 SDRAM Channel a Command Signal Group Ball List

Ball	Signal
AK15	SA_BS0
AK16	SA_BS1
AL21	SA_BS2
AN15	SA_CAS#
AP16	SA_RAS#
AP15	SA_WE#
AL17	SA_MA0
AP17	SA_MA1

Ball	Signal
AP18	SA_MA2
AM17	SA_MA3
AN18	SA_MA4
AM18	SA_MA5
AL19	SA_MA6
AP20	SA_MA7
AM19	SA_MA8
AL20	SA_MA9

Ball	Signal
AM16	SA_MA10
AN20	SA_MA11
AM20	SA_MA12
AM15	SA_MA13
AF29	SA_RCVENIN#
AF28	SA_RCVENOUT#

Table 13-7. DDR / DDR2 SDRAM Channel A Data Signal Group Ball List

Ball	Signal
AG35	SA_DQ0
AH35	SA_DQ1
AL35	SA_DQ2
AL37	SA_DQ3
AH36	SA_DQ4
AJ35	SA_DQ5
AK37	SA_DQ6
AL34	SA_DQ7
AJ37	SA_DM0
AK36	SA_DQS0
AK35	SA_DQS0#
AM36	SA_DQ8
AN35	SA_DQ9
AP32	SA_DQ10
AM31	SA_DQ11
AM34	SA_DQ12
AM35	SA_DQ13
AL32	SA_DQ14
AM32	SA_DQ15
AP35	SA_DM1
AP33	SA_DQS1
AP34	SA_DQS1#
AN31	SA_DQ16
AP31	SA_DQ17
AN28	SA_DQ18
AP28	SA_DQ19
AL30	SA_DQ20
AM30	SA_DQ21
AM28	SA_DQ22
AL28	SA_DQ23
AL29	SA_DM2
AN29	SA_DQS2
AN30	SA_DQS2#
AP27	SA_DQ24
AM27	SA_DQ25
AM23	SA_DQ26
AM22	SA_DQ27
AL23	SA_DQ28
AM24	SA_DQ29
AN22	SA_DQ30
AP22	SA_DQ31
AP24	SA_DM3
AP23	SA_DQS3
AN23	SA_DQS3#
AM9	SA_DQ32
AL9	SA_DQ33
AL6	SA_DQ34
AP7	SA_DQ35
AP11	SA_DQ36
AP10	SA_DQ37
AL7	SA_DQ38
AM7	SA_DQ39
AP9	SA_DM4
AM8	SA_DQS4
AN8	SA_DQS4#
AN5	SA_DQ40
AN6	SA_DQ41
AN3	SA_DQ42
AP3	SA_DQ43
AP6	SA_DQ44
AM6	SA_DQ45
AL4	SA_DQ46
AM3	SA_DQ47
AP4	SA_DM5
AM4	SA_DQS5
AM5	SA_DQS5#
AK2	SA_DQ48
AK3	SA_DQ49
AG2	SA_DQ50
AG1	SA_DQ51
AL3	SA_DQ52
AM2	SA_DQ53
AH3	SA_DQ54
AG3	SA_DQ55
AJ2	SA_DM6
AJ1	SA_DQS6
AH1	SA_DQS6#
AF3	SA_DQ56
AE3	SA_DQ57
AD6	SA_DQ58
AC4	SA_DQ59
AF2	SA_DQ60
AF1	SA_DQ61
AD4	SA_DQ62
AD5	SA_DQ63
AD3	SA_DM7
AE5	SA_DQS7
AE4	SA_DQS7#

Table 13-8.DDR / DDR2 SDRAM Channel B Signal Group Ball List

Ball	Signal		Ball	Signal	Ball	Signal
AJ15	SB_BS0		AH18	SB_MA2	AJ16	SB_MA10
AG17	SB_BS1		AJ18	SB_MA3	AG18	SB_MA11
AG21	SB_BS2		AK18	SB_MA4	AG20	SB_MA12
AK14	SB_RAS#		AJ19	SB_MA5	AG15	SB_MA13
AH14	SB_CAS#		AK19	SB_MA6	AF15	SB_RCVENIN#
AH16	SB_WE#		AH19	SB_MA7	AF14	SB_RCVENOUT#
AH17	SB_MA0		AJ20	SB_MA8		
AK17	SB_MA1		AH20	SB_MA9		

Table 13-9. DDR / DDR2 SDRAM Channel B Signal Group Ball List

Ball	Signal	Ball	Signal	Ball	Signal
AE31	SB_DQ0	AJ28	SB_DQS2	AJ5	SB_DQ46
AE32	SB_DQ1	AK28	SB_DQS2#	AK4	SB_DQ47
AG32	SB_DQ2			AK5	SB_DM5
AG36	SB_DQ3	AF24	SB_DQ24	AH6	SB_DQS5
AE34	SB_DQ4	AG23	SB_DQ25	AH7	SB_DQS5#
AE33	SB_DQ5	AJ22	SB_DQ26	AG5	SB_DQ48
AF31	SB_DQ6	AK22	SB_DQ27	AG4	SB_DQ49
AF30	SB_DQ7	AH24	SB_DQ28	AD8	SB_DQ50
AF32	SB_DM0	AH23	SB_DQ29	AD9	SB_DQ51
AF34	SB_DQS0	AG22	SB_DQ30	AH4	SB_DQ52
AF35	SB_DQS0#	AJ21	SB_DQ31	AG6	SB_DQ53
		AK24	SB_DM3	AE8	SB_DQ54
AH33	SB_DQ8	AK23	SB_DQS3	AD7	SB_DQ55
AH32	SB_DQ9	AJ23	SB_DQS3#	AE7	SB_DM6
AK31	SB_DQ10	AG10	SB_DQ32	AF8	SB_DQS6
AG30	SB_DQ11	AG9	SB_DQ33	AF7	SB_DQS6#
AG34	SB_DQ12	AG8	SB_DQ34		
AG33	SB_DQ13	AH8	SB_DQ35	AC5	SB_DQ56
AH31	SB_DQ14	AH11	SB_DQ36	AB8	SB_DQ57
AJ31	SB_DQ15	AH10	SB_DQ37	AB6	SB_DQ58
AK34	SB_DM1	AJ9	SB_DQ38	AA8	SB_DQ59
AK32	SB_DQS1	AK9	SB_DQ39	AC8	SB_DQ60
AK33	SB_DQS1#	AJ10	SB_DM4	AC7	SB_DQ61
AK30	SB_DQ16	AM10	SB_DQS4	AA4	SB_DQ62
AJ30	SB_DQ17	AL10	SB_DQS4#	AA5	SB_DQ63
AH29	SB_DQ18			AB7	SB_DM7
AH28	SB_DQ19	AJ7	SB_DQ40	AB4	SB_DQS7
AK29	SB_DQ20	AK6	SB_DQ41	AB5	SB_DQS7#
AH30	SB_DQ21	AJ4	SB_DQ42		
AH27	SB_DQ22	AH5	SB_DQ43		
AG28	SB_DQ23	AK8	SB_DQ44		
AK27	SB_DM2	AJ8	SB_DQ45		

Table 13-10. Analog CRT Signal Group

Ball	Signal
A19	RED
B19	RED#
C20	GREEN
B20	GREEN#

Ball	Signal
E21	BLUE
D21	BLUE#
G21	HSYNC
H21	VSYNC

Table 13-11. Analog TV Signal Group

Note: These signals are not supported on the Intel 915GME / Intel 910GMLE chipsets and require termination according to the platform design guide.

Ball	Signal
A15	TVDAC_A
B15	TV_IRTNA
C16	TVDAC_B

Ball	Signal
B16	TV_IRTNB
A17	TVDAC_C
B17	TV_IRTNC

Ball	Signal

Table 13-12. LVDS Display Interface Signal Group

Ball	Signal
B34	LA_DATAN0
B33	LA_DATAN1
B32	LA_DATAN2
B30	LA_CLKN

Ball	Signal
A34	LA_DATAP0
A33	LA_DATAP1
B31	LA_DATAP2
B29	LA_CLKP

Ball	Signal
C29	LB_DATAN0
D28	LB_DATAN1
C27	LB_DATAN2
C25	LB_CLKN

Ball	Signal
C28	LB_DATAP0
D27	LB_DATAP1
C26	LB_DATAP2
C24	LB_CLKP

Table 13-13. LVDS Power Sequencing and Backlight Control Signal Group

Ball	Signal
E25	LBKLT_CRTL
F25	LBKLT_EN
F26	LVDD_EN

Table 13-14. DDC / GMBUS Signal Group

Ball	Signal
E24	DDCCLK
E23	DDCDATA
C23	LCTLA_CLK

Ball	Signal
C22	LCTLB_DATA
F23	LDDC_CLK
F22	LDDC_DATA

Ball	Signal
H25	SDVOCTRL_CLK
H24	SDVOCTRL_DATA

Table 13-15. DMI Serial Interface Signal Group

Ball	Signal
AA31	DMI_RXN0
AB35	DMI_RXN1
AC31	DMI_RXN2
AD35	DMI_RXN3
Y31	DMI_RXP0
AA35	DMI_RXP1

Ball	Signal
AB31	DMI_RXP2
AC35	DMI_RXP3
AA33	DMI_TXN0
AB37	DMI_TXN1
AC33	DMI_TXN2
AD37	DMI_TXN3

Ball	Signal
Y33	DMI_TXP0
AA37	DMI_TXP1
AB33	DMI_TXP2
AC37	DMI_TXP3

Table 13-16. PCI Express Based Graphics / Serial Digital Video Out Receive Signal Group

Ball	PCI Express / Signal	SDVO Signal
E30	EXP_RXN0	SDVO_TVCLKIN#
F34	EXP_RXN1	SDVOB_INT#
G30	EXP_RXN2	SDVO_FLDSTALL#
H34	EXP_RXN3	
J30	EXP_RXN4	
K34	EXP_RXN5	SDVOB_INT#
L30	EXP_RXN6	
M34	EXP_RXN7	
N30	EXP_RXN8	
P34	EXP_RXN9	
R30	EXP_RXN10	
T34	EXP_RXN11	
U30	EXP_RXN12	
V34	EXP_RXN13	
W30	EXP_RXN14	
Y34	EXP_RXN15	

Ball	PCI Express / Signal	SDVO Signal
D30	EXP_RXP0	SDVO_TVCLKIN
E34	EXP_RXP1	SDVOB_INT
F30	EXP_RXP2	SDVO_FLDSTALL
G34	EXP_RXP3	
H30	EXP_RXP4	
J34	EXP_RXP5	SDVOB_INT
K30	EXP_RXP6	
L34	EXP_RXP7	
M30	EXP_RXP8	
N34	EXP_RXP9	
P30	EXP_RXP10	
R34	EXP_RXP11	
T30	EXP_RXP12	
U34	EXP_RXP13	
V30	EXP_RXP14	
W34	EXP_RXP15	

Table 13-17. PCI Express Based Graphics / Serial Digital Video Out Transmit Signal Group

Ball	PCI_E Signal	SDVO Signal
E32	EXP_TXN0	
F36	EXP_TXN1	
G32	EXP_TXN2	
H36	EXP_TXN3	
J32	EXP_TXN4	
K36	EXP_TXN5	
L32	EXP_TXN6	
M36	EXP_TXN7	
N32	EXP_TXN8	
P36	EXP_TXN9	
R32	EXP_TXN10	
T36	EXP_TXN11	
U32	EXP_TXN12	
V36	EXP_TXN13	
W32	EXP_TXN14	
Y36	EXP_TXN15	

Ball	PCI_E Signal	SDVO Signal
D32	EXP_TXP0	
E36	EXP_TXP1	
F32	EXP_TXP2	
G36	EXP_TXP3	
H32	EXP_TXP4	
J36	EXP_TXP5	
K32	EXP_TXP6	
L36	EXP_TXP7	
M32	EXP_TXP8	
N36	EXP_TXP9	
P32	EXP_TXP10	
R36	EXP_TXP11	
T32	EXP_TXP12	
U36	EXP_TXP13	
V32	EXP_TXP14	
W36	EXP_TXP15	

Table 13-18. Thermal and Power Sequencing Signal Group

Ball	Signal
AE29	RSTIN#
H10	HCPURST#
AD30	PWROK

Ball	Signal
F5	THRMTRIP#
J21	EXT_TS0#
H22	EXT_TS1#

Ball	Signal
J23	BM_BUSY#

Ball	Signal

Table 13-19. No Connect Signal Group

Ball	Signal
AP37	NC1
AN37	NC2
AP36	NC3
AP2	NC4
AP1	NC5

Ball	Signal
B37	NC9
AN1	NC6
B1	NC7
A2	NC8
A36	NC10

Ball	Signal
A37	NC11

Table 13-20. Configuration & Reserved Signal Group

Ball	Signal
G16	CFG0
H13	CFG1
G14	CFG2
F16	CFG3
F15	CFG4
G15	CFG5
E16	CFG6
D17	CFG7
J16	CFG8
D15	CFG9

Ball	Signal
E15	CFG10
D14	CFG11
E14	CFG12
H12	CFG13
C14	CFG14
H15	CFG15
J15	CFG16
H14	CFG17
G22	CFG18
G23	CFG19

Ball	Signal
D23	CFG20
G25	RSVD21
G24	RSVD22
J17	RSVD23
A31	RSVD24
A30	RSVD25
D26	RSVD26
D25	RSVD27

Table 13-21. Voltage Reference and Compensation Signal Groups

Ball	Signal Name
System Memory	
AF22	SMOCDCOMP0
AF16	SMOCDCOMP1
AK10	SMRCOMPN
AK11	SMRCOMPP
AE27	SMXSLEWIN
AE28	SMXSLEWOUT
AF9	SMYSLEWIN
AF10	SMYSLEWOUT
AF37	SMVREF0
AD1	SMVREF1
Host Interface	
C1	HXRCOMP

Ball	Signal Name
C2	HXSCOMP
D1	HXSWING
T1	HYRCOMP
L1	HYSCOMP
P1	HYSWING
J11	HVREF
PCI Express/SDVO	
D36	EXP_COMPI
D34	EXP_ICOMPO
CRT DAC	
J20	REFSET
TV	
J18	TV_REFSET

Ball	Signal Name
LVDS	
F28	LVREFH
F27	LVREFL
C33	LIBG
C31	LVBG

Table 13-22. Power Signal Group

Ball	Signal
PLL Signal Group	
AA1	VCCA_HPLL
AA2	VCCA_MPLL
AC2	VCCD_HMPLL1
AC1	VCCD_HMPLL2
Y29	VCCA_3GPLL
Y28	VCCA_3GPLL
Y27	VCCA_3GPLL
B23	VCCA_DPLLA
C35	VCCA_DPLLB
PCI Express Graphics	
AE37	VCC3G
W37	VCC3G
U37	VCC3G
R37	VCC3G
N37	VCC3G
L37	VCC3G
J37	VCC3G

Ball	Signal
F37	VCCA_3GBG
G37	**VSSA_3GBG**
High Voltage	
B22	VCCHV
B21	VCCHV
A21	VCCHV
CRT DAC	
H20	VCC_SYNC
F19	VCCA_CRTDAC
E19	VCCA_CRTDAC
G19	VSSA_CRTDAC
LVDS Signal Group	
B26	VCCD_LVDS
B25	VCCD_LVDS
A25	VCCD_LVDS
B28	VCCTX_LVDS
A28	VCCTX_LVDS
A27	VCCTX_LVDS

Ball	Signal
A35	VCCA_LVDS
B36	**VSSALVDS**
TV Out Signal Group (These signals are not supported on the Intel 915GME / Intel 910GMLE chipsets and require termination according to the platform design guide.)	
D19	VCCD_TVDAC
H17	VCCDQ_TVDAC
F17	VCCA_TVDACA
E17	VCCA_TVDACA
D18	VCCA_TVDACB
C18	VCCA_TVDACB
F18	VCCA_TVDACC
E18	VCCA_TVDACC
H18	VCCA_TVBG
G18	**VSSA_TVBG**

Table 13-23. System Memory Analog Power Signal Group

Ball	Signal
AF20	VCCASM
AP19	VCCASM
AF19	VCCASM
AF18	VCCASM

Table 13-24. System Memory Power Signal Group

Ball	Signal
AB9	VCCSM
AD28	VCCSM
AE1	VCCSM
AE12	VCCSM
AE26	VCCSM
AF12	VCCSM
AF13	VCCSM
AF25	VCCSM
AF26	VCCSM
AG12	VCCSM
AG13	VCCSM
AG25	VCCSM
AG26	VCCSM
AH12	VCCSM
AH13	VCCSM
AH25	VCCSM
AH26	VCCSM
AH37	VCCSM
AJ12	VCCSM
AJ13	VCCSM
AJ25	VCCSM
AJ26	VCCSM
AK12	VCCSM

Ball	Signal
AK13	VCCSM
AK25	VCCSM
AK26	VCCSM
AL12	VCCSM
AL13	VCCSM
AL25	VCCSM
AL26	VCCSM
AM1	VCCSM
AM12	VCCSM
AM13	VCCSM
AM25	VCCSM
AM26	VCCSM
AM37	VCCSM
AN12	VCCSM
AN13	VCCSM
AN25	VCCSM
AN26	VCCSM
AP12	VCCSM
AP13	VCCSM
AP25	VCCSM
AP26	VCCSM
AP29	VCCSM
AP8	VCCSM

Ball	Signal
AB10	VCCSM
AB11	VCCSM
AC11	VCCSM
AC27	VCCSM
AD11	VCCSM
AD27	VCCSM
AE13	VCCSM
AE14	VCCSM
AE15	VCCSM
AE16	VCCSM
AE17	VCCSM
AE18	VCCSM
AE19	VCCSM
AE20	VCCSM
AE21	VCCSM
AE22	VCCSM
AE23	VCCSM
AE24	VCCSM
AE25	VCCSM

Table 13-25. VTT Power Signal Group

Ball	Signal
A6	VTT
B2	VTT
G1	VTT
J10	VTT
J13	VTT
J9	VTT
K10	VTT
K11	VTT
K12	VTT
L9	VTT
M1	VTT
M10	VTT
M2	VTT
M3	VTT
M4	VTT
M5	VTT
M6	VTT
M7	VTT

Ball	Signal
M8	VTT
M9	VTT
N1	VTT
N2	VTT
N3	VTT
N4	VTT
N5	VTT
N6	VTT
N7	VTT
N8	VTT
N9	VTT
P9	VTT
R9	VTT
U9	VTT
V1	VTT
W9	VTT
Y9	VTT
K13	VTT

Ball	Signal
L11	VTT
M11	VTT
N10	VTT
N11	VTT
P10	VTT
P11	VTT
R10	VTT
R11	VTT
T10	VTT
T11	VTT
U10	VTT
U11	VTT
V10	VTT
V11	VTT
W10	VTT
W11	VTT

Table 13-26. GMCH Core Voltage Power Signal Group

Ball	Signal
G28	VCC
H26	VCC
H27	VCC
H28	VCC
J25	VCC
J27	VCC
J28	VCC
J29	VCC
K26	VCC
K27	VCC
K28	VCC
K29	VCC
L28	VCC
M28	VCC
M29	VCC
N29	VCC
R29	VCC

Ball	Signal
T18	VCC
T20	VCC
T29	VCC
U19	VCC
U20	VCC
V18	VCC
V19	VCC
W18	VCC
W20	VCC
P27	VCC
P28	VCC
R27	VCC
R28	VCC
T27	VCC
T28	VCC
U27	VCC
U28	VCC

Ball	Signal
V27	VCC
V28	VCC
K17	VCC
K18	VCC
K19	VCC
K20	VCC
K21	VCC
K22	VCC
K23	VCC
K24	VCC
K25	VCC
L27	VCC
M27	VCC
N27	VCC
N28	VCC

Table 13-27. GMCH Ground Signal Group

Ball	Signal
A14	VSS
A16	VSS
A18	VSS
A20	VSS
A22	VSS
A26	VSS
A29	VSS
A3	VSS
A32	VSS
A9	VSS
AA29	VSS
AA3	VSS
AA30	VSS
AA32	VSS
AA34	VSS
AA36	VSS
AA6	VSS
AA7	VSS
AA9	VSS
AB3	VSS
AB30	VSS
AB32	VSS
AB34	VSS
AB36	VSS
AC28	VSS
AC3	VSS
AC30	VSS
AC32	VSS
AC34	VSS
AC36	VSS
AC6	VSS
AC9	VSS
AD2	VSS
AD29	VSS
AD31	VSS
AD32	VSS
AD33	VSS
AD34	VSS
AD36	VSS
AE2	VSS
AE30	VSS
AE35	VSS
AE36	VSS
AE6	VSS
AE9	VSS
AF11	VSS
AF17	VSS
AF21	VSS
AF23	VSS
AF27	VSS
AF33	VSS
AF36	VSS
AF4	VSS
AG11	VSS
AG14	VSS
AG19	VSS
AG24	VSS
AG27	VSS
AG29	VSS
AG31	VSS
AG37	VSS
AG7	VSS
AH2	VSS
AH22	VSS
AH34	VSS
AH9	VSS
AJ11	VSS
AJ14	VSS
AJ17	VSS
AJ24	VSS
AJ27	VSS
AJ29	VSS
AJ3	VSS
AJ32	VSS
AJ36	VSS
AJ6	VSS
AK20	VSS
AK7	VSS
AL11	VSS
AL14	VSS
AL16	VSS
AL18	VSS
AL2	VSS
AL22	VSS
AL24	VSS
AL27	VSS
AL31	VSS
AL33	VSS
AL36	VSS
AL5	VSS
AL8	VSS
AM29	VSS
AN11	VSS
AN14	VSS
AN17	VSS
AN19	VSS
AN2	VSS
AN21	VSS
AN24	VSS
AN27	VSS
AN32	VSS
AN34	VSS
AN36	VSS
AN4	VSS
AN7	VSS
AN9	VSS
AP30	VSS
AP5	VSS

Ball	Signal
B12	VSS
B14	VSS
B18	VSS
B24	VSS
B27	VSS
B35	VSS
B6	VSS
C15	VSS
C17	VSS
C19	VSS
C21	VSS
C3	VSS
C30	VSS
C32	VSS
C34	VSS
C36	VSS
C4	VSS
C8	VSS
D10	VSS
D12	VSS
D16	VSS
D2	VSS
D20	VSS
D22	VSS
D24	VSS
D29	VSS
D31	VSS
D33	VSS
D35	VSS
E20	VSS
E22	VSS
E26	VSS
E27	VSS
E28	VSS
E29	VSS
E31	VSS

Ball	Signal
E33	VSS
E35	VSS
E37	VSS
E5	VSS
E8	VSS
F11	VSS
F14	VSS
F20	VSS
F21	VSS
F24	VSS
F29	VSS
F31	VSS
F33	VSS
F35	VSS
G17	VSS
G2	VSS
G20	VSS
G26	VSS
G27	VSS
G29	VSS
G31	VSS
G33	VSS
G35	VSS
G7	VSS
H11	VSS
H16	VSS
H19	VSS
H23	VSS
H29	VSS
H31	VSS
H33	VSS
H35	VSS
H37	VSS
H4	VSS
H9	VSS
J12	VSS

Ball	Signal
J14	VSS
J19	VSS
J2	VSS
J22	VSS
J24	VSS
J26	VSS
J31	VSS
J33	VSS
J35	VSS
J6	VSS
K37	VSS
K9	VSS
L10	VSS
L2	VSS
L29	VSS
L31	VSS
L33	VSS
L35	VSS
L4	VSS
L6	VSS
L8	VSS
M31	VSS
M33	VSS
M35	VSS
M37	VSS
N31	VSS
N33	VSS
N35	VSS
P2	VSS
P29	VSS
P31	VSS
P33	VSS
P35	VSS
P37	VSS
P4	VSS
P6	VSS

Ball	Signal
P8	VSS
R31	VSS
R33	VSS
R35	VSS
T19	VSS
T2	VSS
T31	VSS
T33	VSS
T35	VSS
T37	VSS
T6	VSS
T9	VSS
U18	VSS
U29	VSS
U31	VSS
U33	VSS
U35	VSS
U4	VSS
V2	VSS

Ball	Signal
V20	VSS
V31	VSS
V33	VSS
V35	VSS
V37	VSS
V7	VSS
V9	VSS
W19	VSS
W29	VSS
W31	VSS
W33	VSS
W35	VSS
W5	VSS
Y1	VSS
Y30	VSS
Y32	VSS
Y35	VSS
Y37	VSS
Y4	VSS

Ball	Signal
Y8	VSS
AA10	VSS
AA11	VSS
AA27	VSS
AA28	VSS
AB27	VSS
AB28	VSS
K14	VSS
K15	VSS
K16	VSS
K31	VSS
K33	VSS
K35	VSS
V29	VSS
W27	VSS
W28	VSS
Y10	VSS
Y11	VSS

Table 13-28. VCC Core Non-Critical to Function Signal Group

Ball	Signal
L17	VCC_NCTF
L18	VCC_NCTF
L19	VCC_NCTF
L20	VCC_NCTF
L21	VCC_NCTF
L22	VCC_NCTF
L23	VCC_NCTF
L24	VCC_NCTF
L25	VCC_NCTF
L26	VCC_NCTF
M17	VCC_NCTF
M18	VCC_NCTF
M19	VCC_NCTF
M20	VCC_NCTF
M21	VCC_NCTF
M22	VCC_NCTF
M23	VCC_NCTF
M24	VCC_NCTF
M25	VCC_NCTF
M26	VCC_NCTF
N17	VCC_NCTF
N18	VCC_NCTF
N19	VCC_NCTF
N20	VCC_NCTF
N21	VCC_NCTF
N22	VCC_NCTF
N23	VCC_NCTF
N24	VCC_NCTF
N25	VCC_NCTF
N26	VCC_NCTF
P17	VCC_NCTF
P18	VCC_NCTF
P19	VCC_NCTF
P20	VCC_NCTF
P21	VCC_NCTF
P22	VCC_NCTF
P23	VCC_NCTF
P24	VCC_NCTF
P25	VCC_NCTF
P26	VCC_NCTF
R18	VCC_NCTF
R19	VCC_NCTF
R20	VCC_NCTF
R22	VCC_NCTF
R23	VCC_NCTF
R24	VCC_NCTF
R25	VCC_NCTF
R26	VCC_NCTF
T17	VCC_NCTF
T21	VCC_NCTF
T22	VCC_NCTF
T23	VCC_NCTF
T24	VCC_NCTF
T25	VCC_NCTF
T26	VCC_NCTF
U17	VCC_NCTF
U21	VCC_NCTF
U22	VCC_NCTF
U23	VCC_NCTF
U24	VCC_NCTF
U25	VCC_NCTF
U26	VCC_NCTF
V17	VCC_NCTF
V21	VCC_NCTF
V22	VCC_NCTF
V23	VCC_NCTF
V24	VCC_NCTF
V25	VCC_NCTF
V26	VCC_NCTF
W17	VCC_NCTF
W21	VCC_NCTF
W22	VCC_NCTF
W23	VCC_NCTF
W24	VCC_NCTF
W25	VCC_NCTF
W26	VCC_NCTF
Y18	VCC_NCTF
Y19	VCC_NCTF
Y20	VCC_NCTF

Table 13-29. VTT Core Non-Critical to Function Signal Group

Ball	Signal
L12	VTT_NCTF
L13	VTT_NCTF
M12	VTT_NCTF
M13	VTT_NCTF
N12	VTT_NCTF
N13	VTT_NCTF
P12	VTT_NCTF
P13	VTT_NCTF
R12	VTT_NCTF
R13	VTT_NCTF
T12	VTT_NCTF
T13	VTT_NCTF
U12	VTT_NCTF
U13	VTT_NCTF
V12	VTT_NCTF
V13	VTT_NCTF
W12	VTT_NCTF
W13	VTT_NCTF

Table 13-30. VCCSM Non-Critical to Function Signal Group

Ball	Signal
AB12	VCCSM_NCTF
AB13	VCCSM_NCTF
AC12	VCCSM_NCTF
AC13	VCCSM_NCTF
AC14	VCCSM_NCTF
AC15	VCCSM_NCTF
AC16	VCCSM_NCTF
AC17	VCCSM_NCTF
AC18	VCCSM_NCTF
AC19	VCCSM_NCTF
AC20	VCCSM_NCTF

Ball	Signal
AC21	VCCSM_NCTF
AC22	VCCSM_NCTF
AC23	VCCSM_NCTF
AC24	VCCSM_NCTF
AC25	VCCSM_NCTF
AC26	VCCSM_NCTF
AD12	VCCSM_NCTF
AD13	VCCSM_NCTF
AD14	VCCSM_NCTF
AD15	VCCSM_NCTF
AD16	VCCSM_NCTF

Ball	Signal
AD17	VCCSM_NCTF
AD18	VCCSM_NCTF
AD19	VCCSM_NCTF
AD20	VCCSM_NCTF
AD21	VCCSM_NCTF
AD22	VCCSM_NCTF
AD23	VCCSM_NCTF
AD24	VCCSM_NCTF
AD25	VCCSM_NCTF
AD26	VCCSM_NCTF

Table 13-31. VSS Non-Critical to Function Signal Group

Ball	Signal
AA12	VSS_NCTF
AA13	VSS_NCTF
AA14	VSS_NCTF
AA15	VSS_NCTF
AA16	VSS_NCTF
AA17	VSS_NCTF
AA18	VSS_NCTF
AA19	VSS_NCTF
AA20	VSS_NCTF
AA21	VSS_NCTF
AA22	VSS_NCTF
AA23	VSS_NCTF
AA24	VSS_NCTF
AA25	VSS_NCTF
AA26	VSS_NCTF
AB14	VSS_NCTF
AB15	VSS_NCTF
AB16	VSS_NCTF
AB17	VSS_NCTF
AB18	VSS_NCTF
AB19	VSS_NCTF
AB20	VSS_NCTF
AB21	VSS_NCTF
AB22	VSS_NCTF

Ball	Signal
AB23	VSS_NCTF
AB24	VSS_NCTF
AB25	VSS_NCTF
AB26	VSS_NCTF
L14	VSS_NCTF
L15	VSS_NCTF
L16	VSS_NCTF
M14	VSS_NCTF
M15	VSS_NCTF
M16	VSS_NCTF
N14	VSS_NCTF
N15	VSS_NCTF
N16	VSS_NCTF
P14	VSS_NCTF
P15	VSS_NCTF
P16	VSS_NCTF
R14	VSS_NCTF
R15	VSS_NCTF
R16	VSS_NCTF
R17	VSS_NCTF
R21	VSS_NCTF
T14	VSS_NCTF
T15	VSS_NCTF

Ball	Signal
T16	VSS_NCTF
U14	VSS_NCTF
U15	VSS_NCTF
U16	VSS_NCTF
V14	VSS_NCTF
V15	VSS_NCTF
V16	VSS_NCTF
W14	VSS_NCTF
W15	VSS_NCTF
W16	VSS_NCTF
Y12	VSS_NCTF
Y13	VSS_NCTF
Y14	VSS_NCTF
Y15	VSS_NCTF
Y16	VSS_NCTF
Y17	VSS_NCTF
Y21	VSS_NCTF
Y22	VSS_NCTF
Y23	VSS_NCTF
Y24	VSS_NCTF
Y25	VSS_NCTF
Y26	VSS_NCTF

13.2 GMCH Signal Name Ordering Ball list

Table 13-32 applies to the Mobile Intel 915GM/GME/PM and Intel 910GML/GMLE Express Chipset ball-out. Some signals may be RESERVED depending on chipset configuration used. Please refer to the signal description chapter for more details.

Table 13-32. GMCH Signal Name Ordering Ball List

Ball	Signal
E21	BLUE
D21	BLUE#
J23	BM_BUSY#
G16	CFG0
H13	CFG1
G14	CFG2
F16	CFG3
F15	CFG4
G15	CFG5
E16	CFG6
D17	CFG7
J16	CFG8
D15	CFG9
E15	CFG10
D14	CFG11
E14	CFG12
H12	CFG13
C14	CFG14
H15	CFG15
J15	CFG16
H14	CFG17
G22	CFG18
G23	CFG19
D23	CFG20
E24	DDCCLK
E23	DDCDATA
AA31	DMI_RXN0
AB35	DMI_RXN1
AC31	DMI_RXN2
AD35	DMI_RXN3
Y31	DMI_RXP0
AA35	DMI_RXP1
AB31	DMI_RXP2
AC35	DMI_RXP3
AA33	DMI_TXN0
AB37	DMI_TXN1
AC33	DMI_TXN2
AD37	DMI_TXN3
Y33	DMI_TXP0
AA37	DMI_TXP1
AB33	DMI_TXP2
AC37	DMI_TXP3
A24	DREF_CLKN
A23	DREF_CLKP
C37	DREF_SSCLKN
D37	DREF_SSCLKP
D36	EXP_COMPI
D34	EXP_ICOMPO
E30	EXP_RXN0
F34	EXP_RXN1
G30	EXP_RXN2
H34	EXP_RXN3
J30	EXP_RXN4
K34	EXP_RXN5
L30	EXP_RXN6
M34	EXP_RXN7
N30	EXP_RXN8
P34	EXP_RXN9
R30	EXP_RXN10
T34	EXP_RXN11
U30	EXP_RXN12
V34	EXP_RXN13
W30	EXP_RXN14
Y34	EXP_RXN15
D30	EXP_RXP0
E34	EXP_RXP1
F30	EXP_RXP2
G34	EXP_RXP3
H30	EXP_RXP4
J34	EXP_RXP5
K30	EXP_RXP6
L34	EXP_RXP7
M30	EXP_RXP8
N34	EXP_RXP9
P30	EXP_RXP10
R34	EXP_RXP11
T30	EXP_RXP12
U34	EXP_RXP13
V30	EXP_RXP14
W34	EXP_RXP15
E32	EXP_TXN0
F36	EXP_TXN1
G32	EXP_TXN2
H36	EXP_TXN3
J32	EXP_TXN4
K36	EXP_TXN5
L32	EXP_TXN6
M36	EXP_TXN7
N32	EXP_TXN8
P36	EXP_TXN9
R32	EXP_TXN10
T36	EXP_TXN11
U32	EXP_TXN12
V36	EXP_TXN13
W32	EXP_TXN14
Y36	EXP_TXN15
D32	EXP_TXP0
E36	EXP_TXP1
F32	EXP_TXP2
G36	EXP_TXP3
H32	EXP_TXP4
J36	EXP_TXP5
K32	EXP_TXP6
L36	EXP_TXP7
M32	EXP_TXP8
N36	EXP_TXP9
P32	EXP_TXP10
R36	EXP_TXP11
T32	EXP_TXP12

Ball	Signal
U36	EXP_TXP13
V32	EXP_TXP14
W36	EXP_TXP15
J21	EXT_TS0#
H22	EXT_TS1#
AB29	GCLKN
AC29	GCLKP
C20	GREEN
B20	GREEN#
G9	HA3#
C9	HA4#
E9	HA5#
B7	HA6#
A10	HA7#
F9	HA8#
D8	HA9#
B10	HA10#
E10	HA11#
G10	HA12#
D9	HA13#
E11	HA14#
F10	HA15#
G11	HA16#
G13	HA17#
C10	HA18#
C11	HA19#
D11	HA20#
C12	HA21#
B13	HA22#
A12	HA23#
F12	HA24#
G12	HA25#
E12	HA26#
C13	HA27#
B11	HA28#
D13	HA29#
A13	HA30#
F13	HA31#
F8	HADS#
B9	HADSTB0#
E13	HADSTB1#
A5	HBNR#
D5	HBPRI#
E7	HBREQ0#
AB1	HCLKN

Ball	Signal
AB2	HCLKP
H10	HCPURST#
G8	HCPUSLP#
E4	HD0#
E1	HD1#
F4	HD2#
H7	HD3#
E2	HD4#
F1	HD5#
E3	HD6#
D3	HD7#
K7	HD8#
F2	HD9#
J7	HD10#
J8	HD11#
H6	HD12#
F3	HD13#
K8	HD14#
H5	HD15#
H1	HD16#
H2	HD17#
K5	HD18#
K6	HD19#
J4	HD20#
G3	HD21#
H3	HD22#
J1	HD23#
L5	HD24#
K4	HD25#
J5	HD26#
P7	HD27#
L7	HD28#
J3	HD29#
P5	HD30#
L3	HD31#
U7	HD32#
V6	HD33#
R6	HD34#
R5	HD35#
P3	HD36#
T8	HD37#
R7	HD38#
R8	HD39#
U8	HD40#
R4	HD41#

Ball	Signal
T4	HD42#
T5	HD43#
R1	HD44#
T3	HD45#
V8	HD46#
U6	HD47#
W6	HD48#
U3	HD49#
V5	HD50#
W8	HD51#
W7	HD52#
U2	HD53#
U1	HD54#
Y5	HD55#
Y2	HD56#
V4	HD57#
Y7	HD58#
W1	HD59#
W3	HD60#
Y3	HD61#
Y6	HD62#
W2	HD63#
C6	HDBSY#
E6	HDEFER#
H8	HDINV0#
K3	HDINV1#
T7	HDINV2#
U5	HDINV3#
G6	HDPWR#
F7	HDRDY#
G4	HDSTBN0#
K1	HDSTBN1#
R3	HDSTBN2#
V3	HDSTBN3#
G5	HDSTBP0#
K2	HDSTBP1#
R2	HDSTBP2#
W4	HDSTBP3#
F6	RSVD32
D4	HHIT#
D6	HHITM#
B3	HLOCK#
A11	RSVD33
A7	HREQ0#

Ball	Signal
D7	HREQ1#
B8	HREQ2#
C7	HREQ3#
A8	HREQ4#
A4	HRS0#
C5	HRS1#
B4	HRS2#
G21	HSYNC
B5	HTRDY#
J11	HVREF
C1	HXRCOMP
C2	HXSCOMP
D1	HXSWING
T1	HYRCOMP
L1	HYSCOMP
P1	HYSWING
B30	LACLKN
B29	LACLKP
B34	LADATAN0
B33	LADATAN1
B32	LADATAN2
A34	LADATAP0
A33	LADATAP1
B31	LADATAP2
C25	LBCLKN
C24	LBCLKP
C29	LBDATAN0
D28	LBDATAN1
C27	LBDATAN2
C28	LBDATAP0
D27	LBDATAP1
C26	LBDATAP2
E25	LBKLT_CRTL
F25	LBKLT_EN
C23	LCTLA_CLK
C22	LCTLB_DATA
F23	LDDC_CLK
F22	LDDC_DATA
C33	LIBG
C31	LVBG
F26	LVDD_EN
F28	LVREFH
F27	LVREFL
AP37	NC1

Ball	Signal
AN37	NC2
AP36	NC3
AP2	NC4
AP1	NC5
AN1	NC6
B1	NC7
A2	NC8
B37	NC9
A36	NC10
A37	NC11
AD30	PWROK
A19	RED
B19	RED#
J20	REFSET
AE29	RSTIN#
G25	RSVD21
G24	RSVD22
J17	RSVD23
A31	RSVD24
A30	RSVD25
D26	RSVD26
D25	RSVD27
AK15	SA_BS0
AK16	SA_BS1
AL21	SA_BS2
AN15	SA_CAS#
AJ37	SA_DM0
AP35	SA_DM1
AL29	SA_DM2
AP24	SA_DM3
AP9	SA_DM4
AP4	SA_DM5
AJ2	SA_DM6
AD3	SA_DM7
AG35	SA_DQ0
AH35	SA_DQ1
AL35	SA_DQ2
AL37	SA_DQ3
AH36	SA_DQ4
AJ35	SA_DQ5
AK37	SA_DQ6
AL34	SA_DQ7
AM36	SA_DQ8
AN35	SA_DQ9

Ball	Signal
AP32	SA_DQ10
AM31	SA_DQ11
AM34	SA_DQ12
AM35	SA_DQ13
AL32	SA_DQ14
AM32	SA_DQ15
AN31	SA_DQ16
AP31	SA_DQ17
AN28	SA_DQ18
AP28	SA_DQ19
AL30	SA_DQ20
AM30	SA_DQ21
AM28	SA_DQ22
AL28	SA_DQ23
AP27	SA_DQ24
AM27	SA_DQ25
AM23	SA_DQ26
AM22	SA_DQ27
AL23	SA_DQ28
AM24	SA_DQ29
AN22	SA_DQ30
AP22	SA_DQ31
AM9	SA_DQ32
AL9	SA_DQ33
AL6	SA_DQ34
AP7	SA_DQ35
AP11	SA_DQ36
AP10	SA_DQ37
AL7	SA_DQ38
AM7	SA_DQ39
AN5	SA_DQ40
AN6	SA_DQ41
AN3	SA_DQ42
AP3	SA_DQ43
AP6	SA_DQ44
AM6	SA_DQ45
AL4	SA_DQ46
AM3	SA_DQ47
AK2	SA_DQ48
AK3	SA_DQ49
AG2	SA_DQ50
AG1	SA_DQ51
AL3	SA_DQ52

Ball	Signal
AM2	SA_DQ53
AH3	SA_DQ54
AG3	SA_DQ55
AF3	SA_DQ56
AE3	SA_DQ57
AD6	SA_DQ58
AC4	SA_DQ59
AF2	SA_DQ60
AF1	SA_DQ61
AD4	SA_DQ62
AD5	SA_DQ63
AK36	SA_DQS0
AK35	SA_DQS0#
AP33	SA_DQS1
AP34	SA_DQS1#
AN29	SA_DQS2
AN30	SA_DQS2#
AP23	SA_DQS3
AN23	SA_DQS3#
AM8	SA_DQS4
AN8	SA_DQS4#
AM4	SA_DQS5
AM5	SA_DQS5#
AJ1	SA_DQS6
AH1	SA_DQS6#
AE5	SA_DQS7
AE4	SA_DQS7#
AL17	SA_MA0
AP17	SA_MA1
AP18	SA_MA2
AM17	SA_MA3
AN18	SA_MA4
AM18	SA_MA5
AL19	SA_MA6
AP20	SA_MA7
AM19	SA_MA8
AL20	SA_MA9
AM16	SA_MA10
AN20	SA_MA11
AM20	SA_MA12
AM15	SA_MA13
AP16	SA_RAS#
AF29	SA_RCVENIN#
AF28	SA_RCVENOUT#

Ball	Signal
AP15	SA_WE#
AJ15	SB_BS0
AG17	SB_BS1
AG21	SB_BS2
AH14	SB_CAS#
AF32	SB_DM0
AK34	SB_DM1
AK27	SB_DM2
AK24	SB_DM3
AJ10	SB_DM4
AK5	SB_DM5
AE7	SB_DM6
AB7	SB_DM7
AE31	SB_DQ0
AE32	SB_DQ1
AG32	SB_DQ2
AG36	SB_DQ3
AE34	SB_DQ4
AE33	SB_DQ5
AF31	SB_DQ6
AF30	SB_DQ7
AH33	SB_DQ8
AH32	SB_DQ9
AK31	SB_DQ10
AG30	SB_DQ11
AG34	SB_DQ12
AG33	SB_DQ13
AH31	SB_DQ14
AJ31	SB_DQ15
AK30	SB_DQ16
AJ30	SB_DQ17
AH29	SB_DQ18
AH28	SB_DQ19
AK29	SB_DQ20
AH30	SB_DQ21
AH27	SB_DQ22
AG28	SB_DQ23
AF24	SB_DQ24
AG23	SB_DQ25
AJ22	SB_DQ26
AK22	SB_DQ27
AH24	SB_DQ28
AH23	SB_DQ29

Ball	Signal
AG22	SB_DQ30
AJ21	SB_DQ31
AG10	SB_DQ32
AG9	SB_DQ33
AG8	SB_DQ34
AH8	SB_DQ35
AH11	SB_DQ36
AH10	SB_DQ37
AJ9	SB_DQ38
AK9	SB_DQ39
AJ7	SB_DQ40
AK6	SB_DQ41
AJ4	SB_DQ42
AH5	SB_DQ43
AK8	SB_DQ44
AJ8	SB_DQ45
AJ5	SB_DQ46
AK4	SB_DQ47
AG5	SB_DQ48
AG4	SB_DQ49
AD8	SB_DQ50
AD9	SB_DQ51
AH4	SB_DQ52
AG6	SB_DQ53
AE8	SB_DQ54
AD7	SB_DQ55
AC5	SB_DQ56
AB8	SB_DQ57
AB6	SB_DQ58
AA8	SB_DQ59
AC8	SB_DQ60
AC7	SB_DQ61
AA4	SB_DQ62
AA5	SB_DQ63
AF34	SB_DQS0
AF35	SB_DQS0#
AK32	SB_DQS1
AK33	SB_DQS1#
AJ28	SB_DQS2
AK28	SB_DQS2#
AK23	SB_DQS3
AJ23	SB_DQS3#
AM10	SB_DQS4

Ball	Signal
AL10	SB_DQS4#
AH6	SB_DQS5
AH7	SB_DQS5#
AF8	SB_DQS6
AF7	SB_DQS6#
AB4	SB_DQS7
AB5	SB_DQS7#
AH17	SB_MA0
AK17	SB_MA1
AH18	SB_MA2
AJ18	SB_MA3
AK18	SB_MA4
AJ19	SB_MA5
AK19	SB_MA6
AH19	SB_MA7
AJ20	SB_MA8
AH20	SB_MA9
AJ16	SB_MA10
AG18	SB_MA11
AG20	SB_MA12
AG15	SB_MA13
AK14	SB_RAS#
AF15	SB_RCVENIN#
AF14	SB_RCVENOUT#
AH16	SB_WE#
H25	SDVOCTRL_CLK
H24	SDVOCTRL_DATA
AM33	SM_CK0
AN33	SM_CK0#
AL1	SM_CK1
AK1	SM_CK1#
AE11	RSVD28
AE10	RSVD29
AJ34	SM_CK3
AJ33	SM_CK3#
AF6	SM_CK4
AF5	SM_CK4#
AC10	RSVD30
AD10	RSVD31
AP21	SM_CKE0
AM21	SM_CKE1
AH21	SM_CKE2
AK21	SM_CKE3
AN16	SM_CS0#

Ball	Signal
AM14	SM_CS1#
AH15	SM_CS2#
AG16	SM_CS3#
AP14	SM_ODT0
AL15	SM_ODT1
AM11	SM_ODT2
AN10	SM_ODT3
AF22	SMOCDCOMP0
AF16	SMOCDCOMP1
AK10	SMRCOMPN
AK11	SMRCOMPP
AF37	SMVREF0
AD1	SMVREF1
AE27	SMXSLEWIN
AE28	SMXSLEWOUT
AF9	SMYSLEWIN
AF10	SMYSLEWOUT
F5	THRMTRIP#
B15	TV_IRTNA
B16	TV_IRTNB
B17	TV_IRTNC
J18	TV_REFSET
A15	TVDAC_A
C16	TVDAC_B
A17	TVDAC_C
G28	VCC
H26	VCC
H27	VCC
H28	VCC
J25	VCC
J27	VCC
J28	VCC
J29	VCC
K17	VCC
K18	VCC
K19	VCC
K20	VCC
K21	VCC
K22	VCC
K23	VCC
K24	VCC
K25	VCC
K26	VCC
K27	VCC

Ball	Signal
K28	VCC
K29	VCC
L27	VCC
L28	VCC
M27	VCC
M28	VCC
M29	VCC
N27	VCC
N28	VCC
N29	VCC
P27	VCC
P28	VCC
R27	VCC
R28	VCC
R29	VCC
T18	VCC
T20	VCC
T27	VCC
T28	VCC
T29	VCC
U19	VCC
U20	VCC
U27	VCC
U28	VCC
V18	VCC
V19	VCC
V27	VCC
V28	VCC
W18	VCC
W20	VCC
L17	VCC_NCTF
L18	VCC_NCTF
L19	VCC_NCTF
L20	VCC_NCTF
L21	VCC_NCTF
L22	VCC_NCTF
L23	VCC_NCTF
L24	VCC_NCTF
L25	VCC_NCTF
L26	VCC_NCTF
M17	VCC_NCTF
M18	VCC_NCTF
M19	VCC_NCTF
M20	VCC_NCTF

Ball	Signal
M21	VCC_NCTF
M22	VCC_NCTF
M23	VCC_NCTF
M24	VCC_NCTF
M25	VCC_NCTF
M26	VCC_NCTF
N17	VCC_NCTF
N18	VCC_NCTF
N19	VCC_NCTF
N20	VCC_NCTF
N21	VCC_NCTF
N22	VCC_NCTF
N23	VCC_NCTF
N24	VCC_NCTF
N25	VCC_NCTF
N26	VCC_NCTF
P17	VCC_NCTF
P18	VCC_NCTF
P19	VCC_NCTF
P20	VCC_NCTF
P21	VCC_NCTF
P22	VCC_NCTF
P23	VCC_NCTF
P24	VCC_NCTF
P25	VCC_NCTF
P26	VCC_NCTF
R18	VCC_NCTF
R19	VCC_NCTF
R20	VCC_NCTF
R22	VCC_NCTF
R23	VCC_NCTF
R24	VCC_NCTF
R25	VCC_NCTF
R26	VCC_NCTF
T17	VCC_NCTF
T21	VCC_NCTF
T22	VCC_NCTF
T23	VCC_NCTF
T24	VCC_NCTF
T25	VCC_NCTF
T26	VCC_NCTF
U17	VCC_NCTF
U21	VCC_NCTF
U22	VCC_NCTF
U23	VCC_NCTF

Ball	Signal
U24	VCC_NCTF
U25	VCC_NCTF
U26	VCC_NCTF
V17	VCC_NCTF
V21	VCC_NCTF
V22	VCC_NCTF
V23	VCC_NCTF
V24	VCC_NCTF
V25	VCC_NCTF
V26	VCC_NCTF
W17	VCC_NCTF
W21	VCC_NCTF
W22	VCC_NCTF
W23	VCC_NCTF
W24	VCC_NCTF
W25	VCC_NCTF
W26	VCC_NCTF
Y18	VCC_NCTF
Y19	VCC_NCTF
Y20	VCC_NCTF
H20	VCC_SYNC
AE37	VCC3G
J37	VCC3G
L37	VCC3G
N37	VCC3G
R37	VCC3G
U37	VCC3G
W37	VCC3G
F37	VCCA_3GBG
Y29	VCCA_3GPLL
Y27	VCCA_3GPLL
Y28	VCCA_3GPLL
E19	VCCA_CRTDAC
F19	VCCA_CRTDAC
B23	VCCA_DPLLA
C35	VCCA_DPLLB
AA1	VCCA_HPLL
A35	VCCA_LVDS
AA2	VCCA_MPLL
AF18	VCCA_SM
AF19	VCCA_SM
AF20	VCCA_SM
AP19	VCCA_SM
H18	VCCA_TVBG
E17	VCCA_TVDACA

Ball	Signal
F17	VCCA_TVDACA
C18	VCCA_TVDACB
D18	VCCA_TVDACB
E18	VCCA_TVDACC
F18	VCCA_TVDACC
AC2	VCCD_HMPLL1
AC1	VCCD_HMPLL2
A25	VCCD_LVDS
B25	VCCD_LVDS
B26	VCCD_LVDS
D19	VCCD_TVDAC
H17	VCCDQ_TVDAC
A21	VCCHV
B21	VCCHV
B22	VCCHV
AB9	VCCSM
AB10	VCCSM
AB11	VCCSM
AC11	VCCSM
AC27	VCCSM
AD11	VCCSM
AD27	VCCSM
AD28	VCCSM
AE1	VCCSM
AE12	VCCSM
AE13	VCCSM
AE14	VCCSM
AE15	VCCSM
AE16	VCCSM
AE17	VCCSM
AE18	VCCSM
AE19	VCCSM
AE20	VCCSM
AE21	VCCSM
AE22	VCCSM
AE23	VCCSM
AE24	VCCSM
AE25	VCCSM
AE26	VCCSM
AF12	VCCSM
AF13	VCCSM
AF25	VCCSM
AF26	VCCSM
AG12	VCCSM
AG13	VCCSM

Ball	Signal
AG25	VCCSM
AG26	VCCSM
AH12	VCCSM
AH13	VCCSM
AH25	VCCSM
AH26	VCCSM
AH37	VCCSM
AJ12	VCCSM
AJ13	VCCSM
AJ25	VCCSM
AJ26	VCCSM
AK12	VCCSM
AK13	VCCSM
AK25	VCCSM
AK26	VCCSM
AL12	VCCSM
AL13	VCCSM
AL25	VCCSM
AL26	VCCSM
AM1	VCCSM
AM12	VCCSM
AM13	VCCSM
AM25	VCCSM
AM26	VCCSM
AM37	VCCSM
AN12	VCCSM
AN13	VCCSM
AN25	VCCSM
AN26	VCCSM
AP8	VCCSM
AP12	VCCSM
AP13	VCCSM
AP25	VCCSM
AP26	VCCSM
AP29	VCCSM
AB12	VCCSM_NCTF
AB13	VCCSM_NCTF
AC12	VCCSM_NCTF
AC13	VCCSM_NCTF
AC14	VCCSM_NCTF
AC15	VCCSM_NCTF
AC16	VCCSM_NCTF
AC17	VCCSM_NCTF
AC18	VCCSM_NCTF

Ball	Signal
AC19	VCCSM_NCTF
AC20	VCCSM_NCTF
AC21	VCCSM_NCTF
AC22	VCCSM_NCTF
AC23	VCCSM_NCTF
AC24	VCCSM_NCTF
AC25	VCCSM_NCTF
AC26	VCCSM_NCTF
AD12	VCCSM_NCTF
AD13	VCCSM_NCTF
AD14	VCCSM_NCTF
AD15	VCCSM_NCTF
AD16	VCCSM_NCTF
AD17	VCCSM_NCTF
AD18	VCCSM_NCTF
AD19	VCCSM_NCTF
AD20	VCCSM_NCTF
AD21	VCCSM_NCTF
AD22	VCCSM_NCTF
AD23	VCCSM_NCTF
AD24	VCCSM_NCTF
AD25	VCCSM_NCTF
AD26	VCCSM_NCTF
A27	VCCTX_LVDS
A28	VCCTX_LVDS
B28	VCCTX_LVDS
A3	VSS
A9	VSS
A14	VSS
A16	VSS
A18	VSS
A20	VSS
A22	VSS
A26	VSS
A29	VSS
A32	VSS
AA3	VSS
AA6	VSS
AA7	VSS
AA9	VSS
AA10	VSS
AA11	VSS
AA27	VSS
AA28	VSS

Ball	Signal
AA29	VSS
AA30	VSS
AA32	VSS
AA34	VSS
AA36	VSS
AB3	VSS
AB27	VSS
AB28	VSS
AB30	VSS
AB32	VSS
AB34	VSS
AB36	VSS
AC3	VSS
AC6	VSS
AC9	VSS
AC28	VSS
AC30	VSS
AC32	VSS
AC34	VSS
AC36	VSS
AD2	VSS
AD29	VSS
AD31	VSS
AD32	VSS
AD33	VSS
AD34	VSS
AD36	VSS
AE2	VSS
AE6	VSS
AE9	VSS
AE30	VSS
AE35	VSS
AE36	VSS
AF4	VSS
AF11	VSS
AF17	VSS
AF21	VSS
AF23	VSS
AF27	VSS
AF33	VSS
AF36	VSS
AG7	VSS
AG11	VSS
AG14	VSS
AG19	VSS

Ball	Signal
AG24	VSS
AG27	VSS
AG29	VSS
AG31	VSS
AG37	VSS
AH2	VSS
AH9	VSS
AH22	VSS
AH34	VSS
AJ3	VSS
AJ6	VSS
AJ11	VSS
AJ14	VSS
AJ17	VSS
AJ24	VSS
AJ27	VSS
AJ29	VSS
AJ32	VSS
AJ36	VSS
AK7	VSS
AK20	VSS
AL2	VSS
AL5	VSS
AL8	VSS
AL11	VSS
AL14	VSS
AL16	VSS
AL18	VSS
AL22	VSS
AL24	VSS
AL27	VSS
AL31	VSS
AL33	VSS
AL36	VSS
AM29	VSS
AN2	VSS
AN4	VSS
AN7	VSS
AN9	VSS
AN11	VSS
AN14	VSS
AN17	VSS
AN19	VSS
AN21	VSS
AN24	VSS

Ball	Signal
AN27	VSS
AN32	VSS
AN34	VSS
AN36	VSS
AP5	VSS
AP30	VSS
B6	VSS
B12	VSS
B14	VSS
B18	VSS
B24	VSS
B27	VSS
B35	VSS
C3	VSS
C4	VSS
C8	VSS
C15	VSS
C17	VSS
C19	VSS
C21	VSS
C30	VSS
C32	VSS
C34	VSS
C36	VSS
D2	VSS
D10	VSS
D12	VSS
D16	VSS
D20	VSS
D22	VSS
D24	VSS
D29	VSS
D31	VSS
D33	VSS
D35	VSS
E5	VSS
E8	VSS
E20	VSS
E22	VSS
E26	VSS
E27	VSS
E28	VSS
E29	VSS
E31	VSS
E33	VSS

Ball	Signal
E35	VSS
E37	VSS
F11	VSS
F14	VSS
F20	VSS
F21	VSS
F24	VSS
F29	VSS
F31	VSS
F33	VSS
F35	VSS
G2	VSS
G7	VSS
G17	VSS
G20	VSS
G26	VSS
G27	VSS
G29	VSS
G31	VSS
G33	VSS
G35	VSS
H4	VSS
H9	VSS
H11	VSS
H16	VSS
H19	VSS
H23	VSS
H29	VSS
H31	VSS
H33	VSS
H35	VSS
H37	VSS
J2	VSS
J6	VSS
J12	VSS
J14	VSS
J19	VSS
J22	VSS
J24	VSS
J26	VSS
J31	VSS
J33	VSS
J35	VSS
K9	VSS
K14	VSS

Ball	Signal
K15	VSS
K16	VSS
K31	VSS
K33	VSS
K35	VSS
K37	VSS
L2	VSS
L4	VSS
L6	VSS
L8	VSS
L10	VSS
L29	VSS
L31	VSS
L33	VSS
L35	VSS
M31	VSS
M33	VSS
M35	VSS
M37	VSS
N31	VSS
N33	VSS
N35	VSS
P2	VSS
P4	VSS
P6	VSS
P8	VSS
P29	VSS
P31	VSS
P33	VSS
P35	VSS
P37	VSS
R31	VSS
R33	VSS
R35	VSS
T2	VSS
T6	VSS
T9	VSS
T19	VSS
T31	VSS
T33	VSS
T35	VSS
T37	VSS
U4	VSS
U18	VSS
U29	VSS

Ball	Signal
U31	VSS
U33	VSS
U35	VSS
V2	VSS
V7	VSS
V9	VSS
V20	VSS
V29	VSS
V31	VSS
V33	VSS
V35	VSS
V37	VSS
W5	VSS
W19	VSS
W27	VSS
W28	VSS
W29	VSS
W31	VSS
W33	VSS
W35	VSS
Y1	VSS
Y4	VSS
Y8	VSS
Y10	VSS
Y11	VSS
Y30	VSS
Y32	VSS
Y35	VSS
Y37	VSS
G37	VSSA_3GBG
G19	VSSA_CRTDAC
B36	VSSA_LVDS
G18	VSSA_TVBG
AA12	VSS_NCTF
AA13	VSS_NCTF
AA14	VSS_NCTF
AA15	VSS_NCTF
AA16	VSS_NCTF
AA17	VSS_NCTF
AA18	VSS_NCTF
AA19	VSS_NCTF
AA20	VSS_NCTF
AA21	VSS_NCTF
AA22	VSS_NCTF
AA23	VSS_NCTF

Ball	Signal
AA24	VSS_NCTF
AA25	VSS_NCTF
AA26	VSS_NCTF
AB14	VSS_NCTF
AB15	VSS_NCTF
AB16	VSS_NCTF
AB17	VSS_NCTF
AB18	VSS_NCTF
AB19	VSS_NCTF
AB20	VSS_NCTF
AB21	VSS_NCTF
AB22	VSS_NCTF
AB23	VSS_NCTF
AB24	VSS_NCTF
AB25	VSS_NCTF
AB26	VSS_NCTF
L14	VSS_NCTF
L15	VSS_NCTF
L16	VSS_NCTF
M14	VSS_NCTF
M15	VSS_NCTF
M16	VSS_NCTF
N14	VSS_NCTF
N15	VSS_NCTF
N16	VSS_NCTF
P14	VSS_NCTF
P15	VSS_NCTF
P16	VSS_NCTF
R14	VSS_NCTF
R15	VSS_NCTF
R16	VSS_NCTF
R17	VSS_NCTF
R21	VSS_NCTF
T14	VSS_NCTF
T15	VSS_NCTF
T16	VSS_NCTF
U14	VSS_NCTF
U15	VSS_NCTF
U16	VSS_NCTF
V14	VSS_NCTF
V15	VSS_NCTF
V16	VSS_NCTF
W14	VSS_NCTF
W15	VSS_NCTF
W16	VSS_NCTF

Ball	Signal
Y12	VSS_NCTF
Y13	VSS_NCTF
Y14	VSS_NCTF
Y15	VSS_NCTF
Y16	VSS_NCTF
Y17	VSS_NCTF
Y21	VSS_NCTF
Y22	VSS_NCTF
Y23	VSS_NCTF
Y24	VSS_NCTF
Y25	VSS_NCTF
Y26	VSS_NCTF
H21	VSYNC
A6	VTT
B2	VTT
G1	VTT
J9	VTT
J10	VTT
J13	VTT
K10	VTT
K11	VTT
K12	VTT
K13	VTT
L9	VTT
L11	VTT
M1	VTT
M2	VTT
M3	VTT

Ball	Signal
M4	VTT
M5	VTT
M6	VTT
M7	VTT
M8	VTT
M9	VTT
M10	VTT
M11	VTT
N1	VTT
N2	VTT
N3	VTT
N4	VTT
N5	VTT
N6	VTT
N7	VTT
N8	VTT
N9	VTT
N10	VTT
N11	VTT
P9	VTT
P10	VTT
P11	VTT
R9	VTT
R10	VTT
R11	VTT
T10	VTT
T11	VTT
U9	VTT

Ball	Signal
U10	VTT
U11	VTT
V1	VTT
V10	VTT
V11	VTT
W9	VTT
W10	VTT
W11	VTT
Y9	VTT
L12	VTT_NCTF
L13	VTT_NCTF
M12	VTT_NCTF
M13	VTT_NCTF
N12	VTT_NCTF
N13	VTT_NCTF
P12	VTT_NCTF
P13	VTT_NCTF
R12	VTT_NCTF
R13	VTT_NCTF
T12	VTT_NCTF
T13	VTT_NCTF
U12	VTT_NCTF
U13	VTT_NCTF
V12	VTT_NCTF
V13	VTT_NCTF
W12	VTT_NCTF
W13	VTT_NCTF

13.2.1 GMCH Numerical Order Ball List

Table 13-33 applies to the Mobile Intel 915GM/GME/PM and Intel 910GML/GMLE Express Chipset ball-out. Some signals may be RESERVED depending on chipset configuration used. Please refer to the signal description chapter for more details.

Table 13-33. GMCH Numerical Order Ball List

Ball	Signal
A2	NC8
A3	VSS
A4	HRS0#
A5	HBNR#
A6	VTT
A7	HREQ0#
A8	HREQ4#
A9	VSS
A10	HA7#
A11	RSVD33
A12	HA23#
A13	HA30#
A14	VSS
A15	TVDAC_A
A16	VSS
A17	TVDAC_C
A18	VSS
A19	RED
A20	VSS
A21	VCCHV
A22	VSS
A23	DREF_CLKP
A24	DREF_CLKN
A25	VCCD_LVDS
A26	VSS
A27	VCCTX_LVDS
A28	VCCTX_LVDS
A29	VSS
A30	RSVD25
A31	RSVD24
A32	VSS
A33	LADATAP1
A34	LADATAP0
A35	VCCA_LVDS
A36	NC10
A37	NC11

Ball	Signal
AA1	VCCA_HPLL
AA2	VCCA_MPLL
AA3	VSS
AA4	SB_DQ62
AA5	SB_DQ63
AA6	VSS
AA7	VSS
AA8	SB_DQ59
AA9	VSS
AA10	VSS
AA11	VSS
AA12	VSS_NCTF
AA13	VSS_NCTF
AA14	VSS_NCTF
AA15	VSS_NCTF
AA16	VSS_NCTF
AA17	VSS_NCTF
AA18	VSS_NCTF
AA19	VSS_NCTF
AA20	VSS_NCTF
AA21	VSS_NCTF
AA22	VSS_NCTF
AA23	VSS_NCTF
AA24	VSS_NCTF
AA25	VSS_NCTF
AA26	VSS_NCTF
AA27	VSS
AA28	VSS
AA29	VSS
AA30	VSS
AA31	DMI_RXN0
AA32	VSS
AA33	DMI_TXN0
AA34	VSS
AA35	DMI_RXP1
AA36	VSS
AA37	DMI_TXP1

Ball	Signal
AB1	HCLKN
AB2	HCLKP
AB3	VSS
AB4	SB_DQS7
AB5	SB_DQS7#
AB6	SB_DQ58
AB7	SB_DM7
AB8	SB_DQ57
AB9	VCCSM
AB10	VCCSM
AB11	VCCSM
AB12	VCCSM_NCTF
AB13	VCCSM_NCTF
AB14	VSS_NCTF
AB15	VSS_NCTF
AB16	VSS_NCTF
AB17	VSS_NCTF
AB18	VSS_NCTF
AB19	VSS_NCTF
AB20	VSS_NCTF
AB21	VSS_NCTF
AB22	VSS_NCTF
AB23	VSS_NCTF
AB24	VSS_NCTF
AB25	VSS_NCTF
AB26	VSS_NCTF
AB27	VSS
AB28	VSS
AB29	GCLKN
AB30	VSS
AB31	DMI_RXP2
AB32	VSS
AB33	DMI_TXP2
AB34	VSS
AB35	DMI_RXN1
AB36	VSS

Ball	Signal
AB37	DMI_TXN1
AC1	VCCD_HMPLL2
AC2	VCCD_HMPLL1
AC3	VSS
AC4	SA_DQ59
AC5	SB_DQ56
AC6	VSS
AC7	SB_DQ61
AC8	SB_DQ60
AC9	VSS
AC10	RSVD30
AC11	VCCSM
AC12	VCCSM_NCTF
AC13	VCCSM_NCTF
AC14	VCCSM_NCTF
AC15	VCCSM_NCTF
AC16	VCCSM_NCTF
AC17	VCCSM_NCTF
AC18	VCCSM_NCTF
AC19	VCCSM_NCTF
AC20	VCCSM_NCTF
AC21	VCCSM_NCTF
AC22	VCCSM_NCTF
AC23	VCCSM_NCTF
AC24	VCCSM_NCTF
AC25	VCCSM_NCTF
AC26	VCCSM_NCTF
AC27	VCCSM
AC28	VSS
AC29	GCLKP
AC30	VSS
AC31	DMI_RXN2
AC32	VSS
AC33	DMI_TXN2
AC34	VSS
AC35	DMI_RXP3
AC36	VSS
AC37	DMI_TXP3
AD1	SMVREF1
AD2	VSS
AD3	SA_DM7
AD4	SA_DQ62
AD5	SA_DQ63
AD6	SA_DQ58
AD7	SB_DQ55

Ball	Signal
AD8	SB_DQ50
AD9	SB_DQ51
AD10	RSVD31
AD11	VCCSM
AD12	VCCSM_NCTF
AD13	VCCSM_NCTF
AD14	VCCSM_NCTF
AD15	VCCSM_NCTF
AD16	VCCSM_NCTF
AD17	VCCSM_NCTF
AD18	VCCSM_NCTF
AD19	VCCSM_NCTF
AD20	VCCSM_NCTF
AD21	VCCSM_NCTF
AD22	VCCSM_NCTF
AD23	VCCSM_NCTF
AD24	VCCSM_NCTF
AD25	VCCSM_NCTF
AD26	VCCSM_NCTF
AD27	VCCSM
AD28	VCCSM
AD29	VSS
AD30	PWROK
AD31	VSS
AD32	VSS
AD33	VSS
AD34	VSS
AD35	DMI_RXN3
AD36	VSS
AD37	DMI_TXN3
AE1	VCCSM
AE2	VSS
AE3	SA_DQ57
AE4	SA_DQS7#
AE5	SA_DQS7
AE6	VSS
AE7	SB_DM6
AE8	SB_DQ54
AE9	VSS
AE10	RSVD29
AE11	RSVD28
AE12	VCCSM
AE13	VCCSM
AE14	VCCSM
AE15	VCCSM

Ball	Signal
AE16	VCCSM
AE17	VCCSM
AE18	VCCSM
AE19	VCCSM
AE20	VCCSM
AE21	VCCSM
AE22	VCCSM
AE23	VCCSM
AE24	VCCSM
AE25	VCCSM
AE26	VCCSM
AE27	SMXSLEWIN
AE28	SMXSLEWOUT
AE29	RSTIN#
AE30	VSS
AE31	SB_DQ0
AE32	SB_DQ1
AE33	SB_DQ5
AE34	SB_DQ4
AE35	VSS
AE36	VSS
AE37	VCC3G
AF1	SA_DQ61
AF2	SA_DQ60
AF3	SA_DQ56
AF4	VSS
AF5	SM_CK4#
AF6	SM_CK4
AF7	SB_DQS6#
AF8	SB_DQS6
AF9	SMYSLEWIN
AF10	SMYSLEWOUT
AF11	VSS
AF12	VCCSM
AF13	VCCSM
AF14	SB_RCVENOUT#
AF15	SB_RCVENIN#
AF16	SMOCDCOMP1
AF17	VSS
AF18	VCCA_SM
AF19	VCCA_SM
AF20	VCCA_SM
AF21	VSS
AF22	SMOCDCOMP0

Ball	Signal
AF23	VSS
AF24	SB_DQ24
AF25	VCCSM
AF26	VCCSM
AF27	VSS
AF28	SA_RCVENOUT#
AF29	SA_RCVENIN#
AF30	SB_DQ7
AF31	SB_DQ6
AF32	SB_DM0
AF33	VSS
AF34	SB_DQS0
AF35	SB_DQS0#
AF36	VSS
AF37	SMVREF0
AG1	SA_DQ51
AG2	SA_DQ50
AG3	SA_DQ55
AG4	SB_DQ49
AG5	SB_DQ48
AG6	SB_DQ53
AG7	VSS
AG8	SB_DQ34
AG9	SB_DQ33
AG10	SB_DQ32
AG11	VSS
AG12	VCCSM
AG13	VCCSM
AG14	VSS
AG15	SB_MA13
AG16	SM_CS3#
AG17	SB_BS1
AG18	SB_MA11
AG19	VSS
AG20	SB_MA12
AG21	SB_BS2
AG22	SB_DQ30
AG23	SB_DQ25
AG24	VSS
AG25	VCCSM
AG26	VCCSM
AG27	VSS
AG28	SB_DQ23
AG29	VSS

Ball	Signal
AG30	SB_DQ11
AG31	VSS
AG32	SB_DQ2
AG33	SB_DQ13
AG34	SB_DQ12
AG35	SA_DQ0
AG36	SB_DQ3
AG37	VSS
AH1	SA_DQS6#
AH2	VSS
AH3	SA_DQ54
AH4	SB_DQ52
AH5	SB_DQ43
AH6	SB_DQS5
AH7	SB_DQS5#
AH8	SB_DQ35
AH9	VSS
AH10	SB_DQ37
AH11	SB_DQ36
AH12	VCCSM
AH13	VCCSM
AH14	SB_CAS#
AH15	SM_CS2#
AH16	SB_WE#
AH17	SB_MA0
AH18	SB_MA2
AH19	SB_MA7
AH20	SB_MA9
AH21	SM_CKE2
AH22	VSS
AH23	SB_DQ29
AH24	SB_DQ28
AH25	VCCSM
AH26	VCCSM
AH27	SB_DQ22
AH28	SB_DQ19
AH29	SB_DQ18
AH30	SB_DQ21
AH31	SB_DQ14
AH32	SB_DQ9
AH33	SB_DQ8
AH34	VSS
AH35	SA_DQ1
AH36	SA_DQ4

Ball	Signal
AH37	VCCSM
AJ1	SA_DQS6
AJ2	SA_DM6
AJ3	VSS
AJ4	SB_DQ42
AJ5	SB_DQ46
AJ6	VSS
AJ7	SB_DQ40
AJ8	SB_DQ45
AJ9	SB_DQ38
AJ10	SB_DM4
AJ11	VSS
AJ12	VCCSM
AJ13	VCCSM
AJ14	VSS
AJ15	SB_BS0
AJ16	SB_MA10
AJ17	VSS
AJ18	SB_MA3
AJ19	SB_MA5
AJ20	SB_MA8
AJ21	SB_DQ31
AJ22	SB_DQ26
AJ23	SB_DQS3#
AJ24	VSS
AJ25	VCCSM
AJ26	VCCSM
AJ27	VSS
AJ28	SB_DQS2
AJ29	VSS
AJ30	SB_DQ17
AJ31	SB_DQ15
AJ32	VSS
AJ33	SM_CK3#
AJ34	SM_CK3
AJ35	SA_DQ5
AJ36	VSS
AJ37	SA_DM0
AK1	SM_CK1#
AK2	SA_DQ48
AK3	SA_DQ49
AK4	SB_DQ47
AK5	SB_DM5

Ball	Signal
AK6	SB_DQ41
AK7	VSS
AK8	SB_DQ44
AK9	SB_DQ39
AK10	SMRCOMPN
AK11	SMRCOMPP
AK12	VCCSM
AK13	VCCSM
AK14	SB_RAS#
AK15	SA_BS0
AK16	SA_BS1
AK17	SB_MA1
AK18	SB_MA4
AK19	SB_MA6
AK20	VSS
AK21	SM_CKE3
AK22	SB_DQ27
AK23	SB_DQS3
AK24	SB_DM3
AK25	VCCSM
AK26	VCCSM
AK27	SB_DM2
AK28	SB_DQS2#
AK29	SB_DQ20
AK30	SB_DQ16
AK31	SB_DQ10
AK32	SB_DQS1
AK33	SB_DQS1#
AK34	SB_DM1
AK35	SA_DQS0#
AK36	SA_DQS0
AK37	SA_DQ6
AL1	SM_CK1
AL2	VSS
AL3	SA_DQ52
AL4	SA_DQ46
AL5	VSS
AL6	SA_DQ34
AL7	SA_DQ38
AL8	VSS
AL9	SA_DQ33
AL10	SB_DQS4#
AL11	VSS
AL12	VCCSM

Ball	Signal
AL13	VCCSM
AL14	VSS
AL15	SM_ODT1
AL16	VSS
AL17	SA_MA0
AL18	VSS
AL19	SA_MA6
AL20	SA_MA9
AL21	SA_BS2
AL22	VSS
AL23	SA_DQ28
AL24	VSS
AL25	VCCSM
AL26	VCCSM
AL27	VSS
AL28	SA_DQ23
AL29	SA_DM2
AL30	SA_DQ20
AL31	VSS
AL32	SA_DQ14
AL33	VSS
AL34	SA_DQ7
AL35	SA_DQ2
AL36	VSS
AL37	SA_DQ3
AM1	VCCSM
AM2	SA_DQ53
AM3	SA_DQ47
AM4	SA_DQS5
AM5	SA_DQS5#
AM6	SA_DQ45
AM7	SA_DQ39
AM8	SA_DQS4
AM9	SA_DQ32
AM10	SB_DQS4
AM11	SM_ODT2
AM12	VCCSM
AM13	VCCSM
AM14	SM_CS1#
AM15	SA_MA13
AM16	SA_MA10
AM17	SA_MA3
AM18	SA_MA5

Ball	Signal
AM19	SA_MA8
AM20	SA_MA12
AM21	SM_CKE1
AM22	SA_DQ27
AM23	SA_DQ26
AM24	SA_DQ29
AM25	VCCSM
AM26	VCCSM
AM27	SA_DQ25
AM28	SA_DQ22
AM29	VSS
AM30	SA_DQ21
AM31	SA_DQ11
AM32	SA_DQ15
AM33	SM_CK0
AM34	SA_DQ12
AM35	SA_DQ13
AM36	SA_DQ8
AM37	VCCSM
AN1	NC6
AN2	VSS
AN3	SA_DQ42
AN4	VSS
AN5	SA_DQ40
AN6	SA_DQ41
AN7	VSS
AN8	SA_DQS4#
AN9	VSS
AN10	SM_ODT3
AN11	VSS
AN12	VCCSM
AN13	VCCSM
AN14	VSS
AN15	SA_CAS#
AN16	SM_CS0#
AN17	VSS
AN18	SA_MA4
AN19	VSS
AN20	SA_MA11
AN21	VSS
AN22	SA_DQ30
AN23	SA_DQS3#
AN24	VSS

Ball	Signal
AN25	VCCSM
AN26	VCCSM
AN27	VSS
AN28	SA_DQ18
AN29	SA_DQS2
AN30	SA_DQS2#
AN31	SA_DQ16
AN32	VSS
AN33	SM_CK0#
AN34	VSS
AN35	SA_DQ9
AN36	VSS
AN37	NC2
AP1	NC5
AP2	NC4
AP3	SA_DQ43
AP4	SA_DM5
AP5	VSS
AP6	SA_DQ44
AP7	SA_DQ35
AP8	VCCSM
AP9	SA_DM4
AP10	SA_DQ37
AP11	SA_DQ36
AP12	VCCSM
AP13	VCCSM
AP14	SM_ODT0
AP15	SA_WE#
AP16	SA_RAS#
AP17	SA_MA1
AP18	SA_MA2
AP19	VCCA_SM
AP20	SA_MA7
AP21	SM_CKE0
AP22	SA_DQ31
AP23	SA_DQS3
AP24	SA_DM3
AP25	VCCSM
AP26	VCCSM
AP27	SA_DQ24
AP28	SA_DQ19
AP29	VCCSM
AP30	VSS
AP31	SA_DQ17

Ball	Signal
AP32	SA_DQ10
AP33	SA_DQS1
AP34	SA_DQS1#
AP35	SA_DM1
AP36	NC3
AP37	NC1
B1	NC7
B2	VTT
B3	HLOCK#
B4	HRS2#
B5	HTRDY#
B6	VSS
B7	HA6#
B8	HREQ2#
B9	HADSTB0#
B10	HA10#
B11	HA28#
B12	VSS
B13	HA22#
B14	VSS
B15	TV_IRTNA
B16	TV_IRTNB
B17	TV_IRTNC
B18	VSS
B19	RED#
B20	GREEN#
B21	VCCHV
B22	VCCHV
B23	VCCA_DPLLA
B24	VSS
B25	VCCD_LVDS
B26	VCCD_LVDS
B27	VSS
B28	VCCTX_LVDS
B29	LACLKP
B30	LACLKN
B31	LADATAP2
B32	LADATAN2
B33	LADATAN1
B34	LADATAN0
B35	VSS
B36	VSSA_LVDS
B37	NC9
C1	HXRCOMP

Ball	Signal
C2	HXSCOMP
C3	VSS
C4	VSS
C5	HRS1#
C6	HDBSY#
C7	HREQ3#
C8	VSS
C9	HA4#
C10	HA18#
C11	HA19#
C12	HA21#
C13	HA27#
C14	CFG14
C15	VSS
C16	TVDAC_B
C17	VSS
C18	VCCA_TVDACB
C19	VSS
C20	GREEN
C21	VSS
C22	LCTLB_DATA
C23	LCTLA_CLK
C24	LBCLKP
C25	LBCLKN
C26	LBDATAP2
C27	LBDATAN2
C28	LBDATAP0
C29	LBDATAN0
C30	VSS
C31	LVBG
C32	VSS
C33	LIBG
C34	VSS
C35	VCCA_DPLLB
C36	VSS
C37	DREF_SSCLKN
D1	HXSWING
D2	VSS
D3	HD7#
D4	HHIT#
D5	HBPRI#
D6	HHITM#
D7	HREQ1#
D8	HA9#

Ball	Signal
D9	HA13#
D10	VSS
D11	HA20#
D12	VSS
D13	HA29#
D14	CFG11
D15	CFG9
D16	VSS
D17	CFG7
D18	VCCA_TVDACB
D19	VCCD_TVDAC
D20	VSS
D21	BLUE#
D22	VSS
D23	CFG20
D24	VSS
D25	RSVD27
D26	RSVD26
D27	LBDATAP1
D28	LBDATAN1
D29	VSS
D30	EXP_RXP0
D31	VSS
D32	EXP_TXP0
D33	VSS
D34	EXP_ICOMPO
D35	VSS
D36	EXP_COMPI
D37	DREF_SSCLKP
E1	HD1#
E2	HD4#
E3	HD6#
E4	HD0#
E5	VSS
E6	HDEFER#
E7	HBREQ0#
E8	VSS
E9	HA5#
E10	HA11#
E11	HA14#
E12	HA26#
E13	HADSTB1#
E14	CFG12
E15	CFG10
E16	CFG6

Ball	Signal
E17	VCCA_TVDACA
E18	VCCA_TVDACC
E19	VCCA_CRTDAC
E20	VSS
E21	BLUE
E22	VSS
E23	DDCDATA
E24	DDCCLK
E25	LBKLT_CRTL
E26	VSS
E27	VSS
E28	VSS
E29	VSS
E30	EXP_RXN0
E31	VSS
E32	EXP_TXN0
E33	VSS
E34	EXP_RXP1
E35	VSS
E36	EXP_TXP1
E37	VSS
F1	HD5#
F2	HD9#
F3	HD13#
F4	HD2#
F5	THRMTRIP#
F6	RSVD32
F7	HDRDY#
F8	HADS#
F9	HA8#
F10	HA15#
F11	VSS
F12	HA24#
F13	HA31#
F14	VSS
F15	CFG4
F16	CFG3
F17	VCCA_TVDACA
F18	VCCA_TVDACC
F19	VCCA_CRTDAC
F20	VSS
F21	VSS
F22	LDDC_DATA
F23	LDDC_CLK
F24	VSS

Ball	Signal
F25	LBKLT_EN
F26	LVDD_EN
F27	LVREFL
F28	LVREFH
F29	VSS
F30	EXP_RXP2
F31	VSS
F32	EXP_TXP2
F33	VSS
F34	EXP_RXN1
F35	VSS
F36	EXP_TXN1
F37	VCCA_3GBG
G1	VTT
G2	VSS
G3	HD21#
G4	HDSTBN0#
G5	HDSTBP0#
G6	HDPWR#
G7	VSS
G8	HCPUSLP#
G9	HA3#
G10	HA12#
G11	HA16#
G12	HA25#
G13	HA17#
G14	CFG2
G15	CFG5
G16	CFG0
G17	VSS
G18	VSSA_TVBG
G19	VSSA_CRTDAC
G20	VSS
G21	HSYNC
G22	CFG18
G23	CFG19
G24	RSVD22
G25	RSVD21
G26	VSS
G27	VSS
G28	VCC
G29	VSS
G30	EXP_RXN2
G31	VSS
G32	EXP_TXN2

Ball	Signal
G33	VSS
G34	EXP_RXP3
G35	VSS
G36	EXP_TXP3
G37	VSSA_3GBG
H1	HD16#
H2	HD17#
H3	HD22#
H4	VSS
H5	HD15#
H6	HD12#
H7	HD3#
H8	HDINV0#
H9	VSS
H10	HCPURST#
H11	VSS
H12	CFG13
H13	CFG1
H14	CFG17
H15	CFG15
H16	VSS
H17	VCCDQ_TVDAC
H18	VCCA_TVBG
H19	VSS
H20	VCC_SYNC
H21	VSYNC
H22	EXT_TS1#
H23	VSS
H24	SDVOCTRL_DATA
H25	SDVOCTRL_CLK
H26	VCC
H27	VCC
H28	VCC
H29	VSS
H30	EXP_RXP4
H31	VSS
H32	EXP_TXP4
H33	VSS
H34	EXP_RXN3
H35	VSS
H36	EXP_TXN3
H37	VSS
J1	HD23#
J2	VSS

Ball	Signal
J3	HD29#
J4	HD20#
J5	HD26#
J6	VSS
J7	HD10#
J8	HD11#
J9	VTT
J10	VTT
J11	HVREF
J12	VSS
J13	VTT
J14	VSS
J15	CFG16
J16	CFG8
J17	RSVD23
J18	TV_REFSET
J19	VSS
J20	REFSET
J21	EXT_TS0#
J22	VSS
J23	BM_BUSY#
J24	VSS
J25	VCC
J26	VSS
J27	VCC
J28	VCC
J29	VCC
J30	EXP_RXN4
J31	VSS
J32	EXP_TXN4
J33	VSS
J34	EXP_RXP5
J35	VSS
J36	EXP_TXP5
J37	VCC3G
K1	HDSTBN1#
K2	HDSTBP1#
K3	HDINV1#
K4	HD25#
K5	HD18#
K6	HD19#
K7	HD8#
K8	HD14#
K9	VSS

Ball	Signal
K10	VTT
K11	VTT
K12	VTT
K13	VTT
K14	VSS
K15	VSS
K16	VSS
K17	VCC
K18	VCC
K19	VCC
K20	VCC
K21	VCC
K22	VCC
K23	VCC
K24	VCC
K25	VCC
K26	VCC
K27	VCC
K28	VCC
K29	VCC
K30	EXP_RXP6
K31	VSS
K32	EXP_TXP6
K33	VSS
K34	EXP_RXN5
K35	VSS
K36	EXP_TXN5
K37	VSS
L1	HYSCOMP
L2	VSS
L3	HD31#
L4	VSS
L5	HD24#
L6	VSS
L7	HD28#
L8	VSS
L9	VTT
L10	VSS
L11	VTT
L12	VTT_NCTF
L13	VTT_NCTF
L14	VSS_NCTF
L15	VSS_NCTF
L16	VSS_NCTF
L17	VCC_NCTF

Ball	Signal
L18	VCC_NCTF
L19	VCC_NCTF
L20	VCC_NCTF
L21	VCC_NCTF
L22	VCC_NCTF
L23	VCC_NCTF
L24	VCC_NCTF
L25	VCC_NCTF
L26	VCC_NCTF
L27	VCC
L28	VCC
L29	VSS
L30	EXP_RXN6
L31	VSS
L32	EXP_TXN6
L33	VSS
L34	EXP_RXP7
L35	VSS
L36	EXP_TXP7
L37	VCC3G
M1	VTT
M2	VTT
M3	VTT
M4	VTT
M5	VTT
M6	VTT
M7	VTT
M8	VTT
M9	VTT
M10	VTT
M11	VTT
M12	VTT_NCTF
M13	VTT_NCTF
M14	VSS_NCTF
M15	VSS_NCTF
M16	VSS_NCTF
M17	VCC_NCTF
M18	VCC_NCTF
M19	VCC_NCTF
M20	VCC_NCTF
M21	VCC_NCTF
M22	VCC_NCTF
M23	VCC_NCTF
M24	VCC_NCTF
M25	VCC_NCTF

Ball	Signal
M26	VCC_NCTF
M27	VCC
M28	VCC
M29	VCC
M30	EXP_RXP8
M31	VSS
M32	EXP_TXP8
M33	VSS
M34	EXP_RXN7
M35	VSS
M36	EXP_TXN7
M37	VSS
N1	VTT
N2	VTT
N3	VTT
N4	VTT
N5	VTT
N6	VTT
N7	VTT
N8	VTT
N9	VTT
N10	VTT
N11	VTT
N12	VTT_NCTF
N13	VTT_NCTF
N14	VSS_NCTF
N15	VSS_NCTF
N16	VSS_NCTF
N17	VCC_NCTF
N18	VCC_NCTF
N19	VCC_NCTF
N20	VCC_NCTF
N21	VCC_NCTF
N22	VCC_NCTF
N23	VCC_NCTF
N24	VCC_NCTF
N25	VCC_NCTF
N26	VCC_NCTF
N27	VCC
N28	VCC
N29	VCC
N30	EXP_RXN8
N31	VSS
N32	EXP_TXN8
N33	VSS

Ball	Signal
N34	EXP_RXP9
N35	VSS
N36	EXP_TXP9
N37	VCC3G
P1	HYSWING
P2	VSS
P3	HD36#
P4	VSS
P5	HD30#
P6	VSS
P7	HD27#
P8	VSS
P9	VTT
P10	VTT
P11	VTT
P12	VTT_NCTF
P13	VTT_NCTF
P14	VSS_NCTF
P15	VSS_NCTF
P16	VSS_NCTF
P17	VCC_NCTF
P18	VCC_NCTF
P19	VCC_NCTF
P20	VCC_NCTF
P21	VCC_NCTF
P22	VCC_NCTF
P23	VCC_NCTF
P24	VCC_NCTF
P25	VCC_NCTF
P26	VCC_NCTF
P27	VCC
P28	VCC
P29	VSS
P30	EXP_RXP10
P31	VSS
P32	EXP_TXP10
P33	VSS
P34	EXP_RXN9
P35	VSS
P36	EXP_TXN9
P37	VSS
R1	HD44#
R2	HDSTBP2#
R3	HDSTBN2#
R4	HD41#

Ball	Signal
R5	HD35#
R6	HD34#
R7	HD38#
R8	HD39#
R9	VTT
R10	VTT
R11	VTT
R12	VTT_NCTF
R13	VTT_NCTF
R14	VSS_NCTF
R15	VSS_NCTF
R16	VSS_NCTF
R17	VSS_NCTF
R18	VCC_NCTF
R19	VCC_NCTF
R20	VCC_NCTF
R21	VSS_NCTF
R22	VCC_NCTF
R23	VCC_NCTF
R24	VCC_NCTF
R25	VCC_NCTF
R26	VCC_NCTF
R27	VCC
R28	VCC
R29	VCC
R30	EXP_RXN10
R31	VSS
R32	EXP_TXN10
R33	VSS
R34	EXP_RXP11
R35	VSS
R36	EXP_TXP11
R37	VCC3G
T1	HYRCOMP
T2	VSS
T3	HD45#
T4	HD42#
T5	HD43#
T6	VSS
T7	HDINV2#
T8	HD37#
T9	VSS
T10	VTT
T11	VTT
T12	VTT_NCTF

Ball	Signal
T13	VTT_NCTF
T14	VSS_NCTF
T15	VSS_NCTF
T16	VSS_NCTF
T17	VCC_NCTF
T18	VCC
T19	VSS
T20	VCC
T21	VCC_NCTF
T22	VCC_NCTF
T23	VCC_NCTF
T24	VCC_NCTF
T25	VCC_NCTF
T26	VCC_NCTF
T27	VCC
T28	VCC
T29	VCC
T30	EXP_RXP12
T31	VSS
T32	EXP_TXP12
T33	VSS
T34	EXP_RXN11
T35	VSS
T36	EXP_TXN11
T37	VSS
U1	HD54#
U2	HD53#
U3	HD49#
U4	VSS
U5	HDINV3#
U6	HD47#
U7	HD32#
U8	HD40#
U9	VTT
U10	VTT
U11	VTT
U12	VTT_NCTF
U13	VTT_NCTF
U14	VSS_NCTF
U15	VSS_NCTF
U16	VSS_NCTF
U17	VCC_NCTF
U18	VSS
U19	VCC
U20	VCC

Ball	Signal
U21	VCC_NCTF
U22	VCC_NCTF
U23	VCC_NCTF
U24	VCC_NCTF
U25	VCC_NCTF
U26	VCC_NCTF
U27	VCC
U28	VCC
U29	VSS
U30	EXP_RXN12
U31	VSS
U32	EXP_TXN12
U33	VSS
U34	EXP_RXP13
U35	VSS
U36	EXP_TXP13
U37	VCC3G
V1	VTT
V2	VSS
V3	HDSTBN3#
V4	HD57#
V5	HD50#
V6	HD33#
V7	VSS
V8	HD46#
V9	VSS
V10	VTT
V11	VTT
V12	VTT_NCTF
V13	VTT_NCTF
V14	VSS_NCTF
V15	VSS_NCTF
V16	VSS_NCTF
V17	VCC_NCTF
V18	VCC
V19	VCC
V20	VSS
V21	VCC_NCTF
V22	VCC_NCTF
V23	VCC_NCTF
V24	VCC_NCTF
V25	VCC_NCTF
V26	VCC_NCTF
V27	VCC
V28	VCC

Ball	Signal
V29	VSS
V29	VSS
V30	EXP_RXP14
V31	VSS
V32	EXP_TXP14
V33	VSS
V34	EXP_RXN13
V35	VSS
V36	EXP_TXN13
V37	VSS
W1	HD59#
W2	HD63#
W3	HD60#
W4	HDSTBP3#
W5	VSS
W6	HD48#
W7	HD52#
W8	HD51#
W9	VTT
W10	VTT
W11	VTT
W12	VTT_NCTF
W13	VTT_NCTF
W14	VSS_NCTF
W15	VSS_NCTF
W16	VSS_NCTF
W17	VCC_NCTF
W18	VCC

Ball	Signal
W19	VSS
W20	VCC
W21	VCC_NCTF
W22	VCC_NCTF
W23	VCC_NCTF
W24	VCC_NCTF
W25	VCC_NCTF
W26	VCC_NCTF
W27	VSS
W28	VSS
W29	VSS
W30	EXP_RXN14
W31	VSS
W32	EXP_TXN14
W33	VSS
W34	EXP_RXP15
W35	VSS
W36	EXP_TXP15
W37	VCC3G
Y1	VSS
Y2	HD56#
Y3	HD61#
Y4	VSS
Y5	HD55#
Y6	HD62#
Y7	HD58#
Y8	VSS
Y9	VTT

Ball	Signal
Y10	VSS
Y11	VSS
Y12	VSS_NCTF
Y13	VSS_NCTF
Y14	VSS_NCTF
Y15	VSS_NCTF
Y16	VSS_NCTF
Y17	VSS_NCTF
Y18	VCC_NCTF
Y19	VCC_NCTF
Y20	VCC_NCTF
Y21	VSS_NCTF
Y22	VSS_NCTF
Y23	VSS_NCTF
Y24	VSS_NCTF
Y25	VSS_NCTF
Y26	VSS_NCTF
Y27	VCCA_3GPLL
Y28	VCCA_3GPLL
Y29	VCCA_3GPLL
Y30	VSS
Y31	DMI_RXP0
Y32	VSS
Y33	DMI_TXP0
Y34	EXP_RXN15
Y35	VSS
Y36	EXP_TXN15
Y37	VSS

13.3 Mobile Intel 915GMS Express Chipset Ballout Diagram

Figure 13-3. Intel 915GMS GMCH Ballout Diagram

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AL	NC1	NC14	NC16	SA_DQS 1	SA_DQ14	SA_DQ11	SA_DQ24	SA_DQ29	VCCSM	NC	SB_BS2	SB_MA11	SB_MA8	VCCSM	VCCSM	
AK	NC10	VCCSM	VSS	SA_DQS 1#	SA_DQ15	VSS	SA_DQ28	SA_DM3	VSS	NC	VSS	SB_MA7	VSS	VCCSM	VCCSM	
AJ	NC11	SA_DM1	SM_CK3	SM_CK3#	VSS	SA_DQ10	SA_DQ25	SA_DQS 3#	SA_DQS 3	NC	SM_CKE 3	SB_MA6	SB_MA5	VCCSM	VCCSM	
AH											SM_CKE 2	SB_MA9	VSS	VCCSM	VCCSM	
AG	SA_DQ13	SA_DQ12	SA_DQ8	SA_DQ9	SA_DQ26	SA_DQ27	VSS	SA_DQ31	SA_DQ30	NC	VSS	SB_MA12	SB_MA4	VCCSM	VCCSM	
AF	SM_CK0#	VSS	SA_DQ16	VSS	SA_DQ21	SA_DQS 2#	SA_DQS 2	SA_DM2	VSS	NC	SA_MA7	SA_MA6	VSS	VCCSM	VCCSM	
AE	SM_CK0	VSS	SA_DQ3	SA_DQ17	SA_DQ20	VSS	SA_DQ18	SA_DQ19	SA_DQ22	NC	SA_MA8	SA_MA5	SA_MA4	VCCSM	VCCSM	
AD											VSS	SA_MA3	VSS	VCCSM	VCCSM	
AC	VCCSM	SA_DQ7	SA_DQ2	VSS	SA_RCV ENIN#	SA_DQ23	SM_CKE 1	VSS	SM_CKE 0	NC	SA_MA0	SA_MA1	SA_MA2	VCCSM	VCCSM	
AB	SA_DQ6	VSS	SA_DQS 0	VSS	SMOCDC OMP0	SA_RCV ENOUT#	SA_BS2	SA_MA12	SA_MA11	NC	NC	NC	NC	NC	NC	
AA	SA_DM0	SA_DQS 0#	SA_DQ5	SA_DQ4	VSS	VSS	SMXSLE WOUT	SA_MA9	VSS	NC	NC	NC	NC	NC	NC	NC
Y	VSS	SMVREF 0	VSS	SA_DQ1	SA_DQ0	VSS	VSS	SMXSLE WIN	VSS	NC	NC	NC	NC	NC	NC	NC
W	DMI_TXN 1	VSS	DMI_RXN 1	VSS	PWROK	VSS	RSTIN#	VSS	GCLKP	NC	NC	NC	NC	NC	NC	NC
V	DMI_TXP 1	VSS	DMI_RXP 1	VSS	VSS	DMI_TXN 0	VSS	DMI_RXN 0	GCLKN	NC	NC	NC	NC	NC	NC	NC
U	VSS	SDVOB_ BLKN	VSS	SDVO_FL DSTALL#	VSS	DMI_TXP 0	VSS	DMI_RXP 0	VSS	NC	NC	NC	NC	NC	VSS	VCC
T											NC	NC	NC	NC	VCC	VCC
R	VCC3G	SDVOB_ BLKP	VSS	SDVO_FL DSTALL	VSS	VSS	VSS	VSS	VCCA_3 GPLL	NC	NC	NC	NC	NC	VCC	VSS
P	VCC3G	SDVOB_ BLUE#	VSS	SDVO_IN T#	VSS	EXP_CO MPI	VSS	VCC	VSS	NC	NC	NC	NC	NC	NC	NC
N	VSS	EXP_TXP 2	VSS	SDVO_IN T	VSS	SDVOB_G	VSS	VCC	VCC	NC	NC	NC	NC	NC	NC	NC
M	VCCA_3 GBG	SDVOB_ RED#	VSS	SDVO_T VCLKIN#	VSS	SDVOB_ GREEN	VSS	VCC	VSS	NC	NC	NC	NC	NC	NC	NC
L	VSSA_3 GBG	SDVOB_ RED	VSS	SDVO_T VCLKIN	VSS	EXP_ICO MPO	VSS	VCC	VCC	NC	NC	NC	NC	NC	NC	NC
K	NC	NC	NC		NC	NC	NC		NC	NC	NC	NC	NC	NC	NC	
J	DREF_S SCLKP	VCCA_D PLLB	LVREFH		EXT_TSD #	BM_BUS Y#	DDCDAT A		DDCCLK	VSS	REFSET	VSS	TV_REFS ET	THRMTRI P#	VSS	
H	DREF_S SCLKN	VSS	LVREFL		SDVOCT RL_DATA	VSS	LVDD_EN		VSS	HSYNC	VCC_SY NC	VSS	RSVD23	VSS	CFG6	
G	VSS	LVBG	VSS		SDVOCT RL_CLK	LBKLT_C RTL	VSS		VSYNC	VSS	VSS	VCCA_TV DACC	VCCA_TV DACB	VCCA_TV DACA	CFG5	
F	LADATAN 0	LIBG	RSVD24		VSS	LBKLT_E N	LDDC_DA TA		VSS	RED#	RED	VCCA_TV DACC	VCCA_TV DACB	VCCA_TV DACA	VSS	
E	LADATAP 0	VSS	VSS		RSVD25	VSS	LDDC_CL K		VSS	GREEN	VSS	VSSA_TV BG	VCCA_TV BG	VCCD_TV DAC	CFG1	
D	LADATAN 1	LADATAP 1	LADATAN 2		LACLKN	LCTLA_C LK	VSS		BLUE	GREEN#	VCCA_C RTDAC	VSSA_C RTDAC	VSS	VSS	VCCDQ_ TVDAC	
C	NC12	VSS	LADATAP 2		LACLKP	LCTLB_D ATA	VSS		BLUE#	VCCHV	VCCHV	VCCA_C RTDAC	VSS	TVDAC_B	VSS	
B	NC13	VSSALV DS	VCCA_LV DS		VSS	VCCTX_L VDS	VCCD_LV DS		VCCD_LV DS	VSS	VCCA_D PLLA	VCCHV	TV_IRTN C	TV_IRTN B	TV_IRTN A	
A	NC	NC15	NC2		VSS	VCCTX_L VDS	VSS		VCCD_LV DS	DREF_CL KN	DREF_CL KP	VSS	TVDAC_C	VSS	TVDAC_A	
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Figure 13-4. Intel 915GMS GMCH Ballout Diagram

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
VCCA_SM	SM_CS2#	SB_MA13	SA_DQ36	SA_DQ33	SA_DQS4#	SA_DQ35		SA_DQ48	VCCSM	SA_DM6		NC3	NC5	NC6	AL
VSS	SB_WE#	SM_ODT2	VSS	SA_DQ32	SA_DQS4	VSS		SA_DQ49	SA_DQ52	VSS		SA_DQ54	SA_DQ50	NC7	AK
SA_WE#	SB_BS0	SB_CAS#	SM_ODT3	SA_DQ37	SA_DM4	SA_DQ39		SA_DQ34	SA_DQ53	SM_CK4#		VSS	SA_DQ51	NC8	AJ
VSS	SB_RAS#	VSS	SM_CS3#	SA_DQ44	VSS	SA_DQ38		SA_DQ42	VSS	SM_CK4		SA_DQS6	SA_DQ55	SA_DQ56	AH
SA_RAS#	SB_BS1	SM_CS1#	SM_ODT1	SA_DQ45	SA_DQ40	SA_DQS5		SA_DM5	SA_DQ46	SA_DQS6#		VSS	VSS	SA_DQ57	AG
VSS	SB_MA10	SA_MA13	SM_ODT0	VSS	SA_DQ41	SA_DQS5#		VSS	SA_DQ43	SM_CK1		SA_DQ60	SA_DQS7#	VCCSM	AF
SA_BS0	SB_MA1	VSS	SA_CAS#	VSS	VSS	SMOCDCOMP1		SMRCOMPP	SA_DQ47	SM_CK1#		SA_DQ61	SA_DQS7	SMVREF1	AE
VSS	SB_MA3	SA_BS1	VSS	SM_CS0#	SMYSLEWOUT	VSS		SMRCOMPN	SA_DM7	VSS		SA_DQ62	VSS	VCCA_HPLL	AD
SB_MA2	VCCA_SM	VCCA_SM	SB_MA0	SA_MA10	SMYSLEWIN	VSS		SA_DQ59	SA_DQ58	VCCD_HMPLL2		VCCD_HMPLL1	SA_DQ63	VCCA_MPLL	AC
NC	NC	NC	NC	NC	NC	NC		NC	NC	NC		NC	NC	NC	AB
NC	NC	NC	NC	NC	NC	HD55#	HD56#	VSS	HD59#	HDSTBP3#	HDSTBN3#	HCLKN	VSS	HD57#	AA
NC	NC	NC	NC	NC	NC	VSS	HD61#	HD63#	HD60#	HD54#	VSS	HCLKP	HD53#	VTT	Y
NC	NC	NC	NC	NC	NC	HD62#	HD49#	HD48#	VSS	HDINV3#	HD52#	HD40#	RSVD1	HD50#	W
NC	NC	NC	NC	NC	NC	HD27#	VSS	HD58#	HD47#	HD46#	HD33#	HD32#	HD51#	VSS	V
VSS	NC	NC	NC	NC	NC	HD26#	HD24#	VSS	HD44#	HD45#	VSS	HD30#	HDSTBP2#	HDSTBN2#	U
VCC	NC	NC	NC	NC											T
VCC	NC	NC	NC	NC	NC	HD31#	HD37#	HDINV2#	HD34#	HD43#	HD41#	HD42#	HD19#	HD28#	R
NC	NC	NC	NC	NC	NC	HD39#	VSS	HD38#	VSS	HD35#	VSS	HD36#	VSS	HD18#	P
NC	NC	NC	NC	NC	NC	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	N
NC	NC	NC	NC	NC	NC	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	VTT	M
NC	NC	NC	NC	NC	NC	HDSTBP1#	VSS	HDINV1#	VSS	HD23#	VSS	HYSWING	VSS	HYRCOMP	L
NC	NC	NC	NC	NC	NC	HD14#	HDSTBN1#	HD25#	HD29#	HD20#	HD17#	HD16#	HYSCOMP	HXRCOMP	K
HA24#	HA18#	HXSWING	HREQ4#	HVREF	NC	HD8#	HD11#	HD10#	HDINV0#	HD3#	VSS	HD21#	HD22#	HD12#	J
HADSTB1#	HA20#	VSS	HA25#	VSS											H
VSS	HA17#	HA19#	HA16#	HA4#	NC	HADS#	VSS	HD15#	VSS	HDSTBN0#	HDSTBP0#	HD5#	VSS	HDPWR#	G
CFG2	HA28#	HA12#	VSS	HADSTB0#	NC	HBREQ0#	HDBSY#	HCPURST#	HD9#	HD0#	HD6#	HD4#	HD1#	HD13#	F
VSS	HA29#	HA26#	HA5#	HA13#	NC	HTRDY#	HBNR#	VSS	HXSCOMP	HDEFER#	VSS	HD7#	HD2#	VTT	E
CFG0	VSS	HA30#	HA11#	VSS											D
VSS	HA27#	HA23#	HA15#	HA7#	NC	HA9#	VSS	HRS2#	HA3#	HCPUSLP#	HLOCK#	HHITM#	VSS	NC9	C
VSS	HA31#	HA21#	VSS	HA8#	NC	VSS	HA6#	HREQ1#	VSS	HRS1#	VSS	HBPRI#	HHIT#	NC18	B
VSS	HA22#	HA14#	VTT	HA10#	NC	HREQ2#	HREQ0#	HREQ3#	VTT	HRS0#	HDRDY#	NC4	NC17		A
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	

13.4 Mobile Intel 915GMS Series Express Chipset Family Ballout List

Some signals may be RESERVED depending on which Mobile Intel 915GMS Express Chipset configuration used. Please refer to the signal description chapter for more details.

Table 13-34. PLL Signal Group

Ball	Signal
V23	GCLKN
W23	GCLKP
AA3	HCLKN
Y3	HCLKP
A22	DREF_CLKN
A21	DREF_CLKP
H31	DREF_SSCLKN
J31	DREF_SSCLKP

Table 13-35.Host Address Signal Group

Ball	Signal
C6	HA3#
G11	HA4#
E12	HA5#
B8	HA6#
C11	HA7#
B11	HA8#
C9	HA9#
A11	HA10#
D12	HA11#
F13	HA12#
E11	HA13#
A13	HA14#

Ball	Signal
C12	HA15#
G12	HA16#
F11	HADSTB0#
A8	HREQ0#
B7	HREQ1#
A9	HREQ2#
A7	HREQ3#
J12	HREQ4#
G14	HA17#
J14	HA18#
G13	HA19#
H14	HA20#

Ball	Signal
B13	HA21#
A14	HA22#
C13	HA23#
J15	HA24#
H12	HA25#
E13	HA26#
C14	HA27#
F14	HA28#
E14	HA29#
D13	HA30#
B14	HA31#
H15	HADSTB1#

Table 13-36. Host Control Signal Group

Ball	Signal
G9	HADS#
E8	HBNR#
B3	HBPRI#
E9	HTRDY#
A4	HDRDY#
F8	HDBSY#

Ball	Signal
E5	HDEFER#
C4	HLOCK#
F9	HBREQ0#
A5	HRS0#
B5	HRS1#
C7	HRS2#

Ball	Signal
B2	HHIT#
C3	HHITM#
G1	HDPWR#
C5	HSLPCPU#

Table *13-37. Host Data Signal Group*

Ball	Signal
F5	HD0#
F2	HD1#
E2	HD2#
J5	HD3#
F3	HD4#
G3	HD5#
F4	HD6#
E3	HD7#
J9	HD8#
F6	HD9#
J7	HD10#
J8	HD11#
J1	HD12#
F1	HD13#
K9	HD14#
G7	HD15#
J6	HDINV0#
G5	HDSTBN0#
G4	HDSTBP0#
K3	HD16#
K4	HD17#
P1	HD18#
R2	HD19#
K5	HD20#
J3	HD21#
J2	HD22#

Ball	Signal
L5	HD23#
U8	HD24#
K7	HD25#
U9	HD26#
V9	HD27#
R1	HD28#
K6	HD29#
U3	HD30#
R9	HD31#
L7	HDINV1#
K8	HDSTBN1#
L9	HDSTBP1#
V3	HD32#
V4	HD33#
R6	HD34#
P5	HD35#
P3	HD36#
R8	HD37#
P7	HD38#
P9	HD39#
W3	HD40#
R4	HD41#
R3	HD42#
R5	HD43#
U6	HD44#
U5	HD45#

Ball	Signal
V5	HD46#
V6	HD47#
R7	HDINV2#
U1	HDSTBN2#
U2	HDSTBP2#
W7	HD48#
W8	HD49#
W1	HD50#
V2	HD51#
W4	HD52#
Y2	HD53#
Y5	HD54#
AA9	HD55#
AA8	HD56#
AA1	HD57#
V7	HD58#
AA6	HD59#
Y6	HD60#
Y8	HD61#
W9	HD62#
Y7	HD63#
W5	HDINV3#
AA4	HDSTBN3#
AA5	HDSTBP3#

Table 13-38. DDR2 SDRAM Common Signal Group Ball List

Ball	Signal
AE31	SM_CK0
AF31	SM_CK0#
AF5	SM_CK1
AE5	SM_CK1#
AJ29	SM_CK3
AJ28	SM_CK3#
AH5	SM_CK4

Ball	Signal
AJ5	SM_CK4#
AC23	SM_CKE0
AC25	SM_CKE1
AH21	SM_CKE2
AJ21	SM_CKE3
AD11	SM_CS0#
AG13	SM_CS1#

Ball	Signal
AL14	SM_CS2#
AH12	SM_CS3#
AF12	SM_ODT0
AG12	SM_ODT1
AK13	SM_ODT2
AJ12	SM_ODT3

Table 13-39. DDR2 SDRAM Channel a Command Signal Group Ball List

Ball	Signal
AE15	SA_BS0
AD13	SA_BS1
AB25	SA_BS2
AE12	SA_CAS#
AG15	SA_RAS#
AJ15	SA_WE#
AC21	SA_MA0
AC20	SA_MA1

Ball	Signal
AC19	SA_MA2
AD20	SA_MA3
AE19	SA_MA4
AE20	SA_MA5
AF20	SA_MA6
AF21	SA_MA7
AE21	SA_MA8
AA24	SA_MA9

Ball	Signal
AC11	SA_MA10
AB23	SA_MA11
AB24	SA_MA12
AF13	SA_MA13
AC27	SA_RCVENIN#
AB26	SA_RCVENOUT#

Table 13-40. DDR2 SDRAM Channel A Data Signal Group Ball List

Ball	Signal
Y27	SA_DQ0
Y28	SA_DQ1
AC29	SA_DQ2
AE29	SA_DQ3
AA28	SA_DQ4
AA29	SA_DQ5
AB31	SA_DQ6
AC30	SA_DQ7
AA31	SA_DM0
AB29	SA_DQS0
AA30	SA_DQS0#
AG29	SA_DQ8
AG28	SA_DQ9
AJ26	SA_DQ10
AL26	SA_DQ11
AG30	SA_DQ12
AG31	SA_DQ13
AL27	SA_DQ14
AK27	SA_DQ15
AJ30	SA_DM1
AL28	SA_DQS1
AK28	SA_DQS1#
AF29	SA_DQ16
AE28	SA_DQ17
AE25	SA_DQ18
AE24	SA_DQ19
AE27	SA_DQ20
AF27	SA_DQ21
AE23	SA_DQ22
AC26	SA_DQ23

Ball	Signal
AF24	SA_DM2
AF25	SA_DQS2
AF26	SA_DQS2#
AL25	SA_DQ24
AJ25	SA_DQ25
AG27	SA_DQ26
AG26	SA_DQ27
AK25	SA_DQ28
AL24	SA_DQ29
AG23	SA_DQ30
AG24	SA_DQ31
AK24	SA_DM3
AJ23	SA_DQS3
AJ24	SA_DQS3#
AK11	SA_DQ32
AL11	SA_DQ33
AJ7	SA_DQ34
AL9	SA_DQ35
AL12	SA_DQ36
AJ11	SA_DQ37
AH9	SA_DQ38
AJ9	SA_DQ39
AJ10	SA_DM4
AK10	SA_DQS4
AL10	SA_DQS4#
AG10	SA_DQ40
AF10	SA_DQ41
AH7	SA_DQ42
AF6	SA_DQ43
AH11	SA_DQ44

Ball	Signal
AG11	SA_DQ45
AG6	SA_DQ46
AE6	SA_DQ47
AG7	SA_DM5
AG9	SA_DQS5
AF9	SA_DQS5#
AL7	SA_DQ48
AK7	SA_DQ49
AK2	SA_DQ50
AJ2	SA_DQ51
AK6	SA_DQ52
AJ6	SA_DQ53
AK3	SA_DQ54
AH2	SA_DQ55
AL5	SA_DM6
AH3	SA_DQS6
AG5	SA_DQS6#
AH1	SA_DQ56
AG1	SA_DQ57
AC6	SA_DQ58
AC7	SA_DQ59
AF3	SA_DQ60
AE3	SA_DQ61
AD3	SA_DQ62
AC2	SA_DQ63
AD6	SA_DM7
AE2	SA_DQS7
AF2	SA_DQS7#

Table 13-41. DDR2 SDRAM Channel B Signal Group Ball List

Ball	Signal	Ball	Signal	Ball	Signal
AJ14	SB_BS0	AE14	SB_MA1	AL19	SB_MA8
AG14	SB_BS1	AC15	SB_MA2	AH20	SB_MA9
AL21	SB_BS2	AD14	SB_MA3	AF14	SB_MA10
AH14	SB_RAS#	AG19	SB_MA4	AL20	SB_MA11
AJ13	SB_CAS#	AJ19	SB_MA5	AG20	SB_MA12
AK14	SB_WE#	AJ20	SB_MA6	AL13	SB_MA13
AC12	SB_MA0	AK20	SB_MA7		

Table 13-42. Analog CRT Signal Group

Ball	Signal	Ball	Signal	Ball	Signal
F21	RED	D22	GREEN#	H22	HSYNC
F22	RED#	D23	BLUE	G23	VSYNC
E22	GREEN	C23	BLUE#		

Table 13-43. Analog TV Signal Group

Ball	Signal	Ball	Signal	Ball	Signal
A17	TVDAC_A	C18	TVDAC_B	A19	TVDAC_C
B17	TV_IRTNA	B18	TV_IRTNB	B19	TV_IRTNC

Table 13-44. LVDS Display Interface Signal Group

Ball	Signal
E31	LADATAP0
D30	LADATAP1
C29	LADATAP2
C27	LACLKP
F31	LADATAN0
D31	LADATAN1
D29	LADATAN2
D27	LACLKN

Table 13-45. LVDS Power Sequencing and Backlight Control Signal Group

Ball	Signal
G26	LBKLT_CRTL
F26	LBKLT_EN
H25	LVDD_EN

Table 13-46. LVDS Power Sequencing and Backlight Control Signal Group

Ball	Signal
G26	LBKLT_CRTL
F26	LBKLT_EN
H25	LVDD_EN

Table *13-47. DDC / GMBUS Signal Group*

Ball	Signal
J23	DDCCLK
J25	DDCDATA
D26	LCTLA_CLK

Ball	Signal
C26	LCTLB_DATA
E25	LDDC_CLK
F25	LDDC_DATA

Ball	Signal
G27	SDVOCTRL_CLK
H27	SDVOCTRL_DATA

Table 13-48. DMI Serial Interface Signal Group

Ball	Signal
V24	DMI_RXN0
W29	DMI_RXN1
U24	DMI_RXP0
V29	DMI_RXP1

Ball	Signal
V26	DMI_TXN0
W31	DMI_TXN1
U26	DMI_TXP0
V31	DMI_TXP1

Table 13-49. Serial Digital Video Out Receive Signal Group

Ball	SDVO Signal
M28	SDVO_TVCLKIN#
P28	SDVOB_INT#
U28	SDVO_FLDSTALL#

Ball	SDVO Signal
L28	SDVO_TVCLKIN
N28	SDVOB_INT
R28	SDVO_FLDSTALL

Table 13-50. Serial Digital Video Out Transmit Signal Group

Ball	SDVO Signal
M30	SDVOB_RED#
N26	SDVOB_GREEN#
P30	SDVOB_BLUE#
U30	SDVOB_CLKN

Ball	SDVO Signal
L30	SDVOB_RED
M26	SDVOB_GREEN
N30	SDVOB_BLUE
R30	SDVOB_CLKP

Table 13-51. Thermal and Power Sequencing Signal Group

Ball	Signal
W25	RSTIN#
F7	HCPURST#
W27	PWROK
J26	BM_BUSY#
J18	THRMTRIP#
J27	EXT_TS0#

Table 13-52. No Connect Signal Group

Ball	Signal
A10	NC
A2	NC
A29	NC
A3	NC
A30	NC
A31	NC
AA10	NC
AA11	NC
AA12	NC
AA13	NC
AA14	NC
AA15	NC
AA16	NC
AA17	NC
AA18	NC
AA19	NC
AA20	NC
AA21	NC
AA22	NC
AB1	NC
AB10	NC
AB11	NC
AB12	NC
AB13	NC
AB14	NC
AB15	NC
AB17	NC
AB18	NC
AB19	NC
AB2	NC
AB20	NC
AB21	NC
AB22	NC
AB3	NC
AB5	NC
AB6	NC
AB7	NC
AB9	NC
AC22	NC
AE22	NC
AF22	NC
AG22	NC
AJ1	NC
AJ22	NC
AJ31	NC
AK1	NC
AK22	NC
AK31	NC
AL1	NC
AL2	NC
AL22	NC
AL29	NC
AL3	NC
AL30	NC
AL31	NC
B1	NC
B10	NC
B31	NC
C1	NC
C10	NC
C31	NC
E10	NC
F10	NC
G10	NC
J10	NC
K10	NC
K11	NC
K12	NC
K13	NC
K14	NC
K15	NC
K17	NC
K18	NC
K19	NC
K20	NC
K21	NC
K22	NC
K23	NC
K25	NC
K26	NC
K27	NC
K29	NC
K30	NC
K31	NC
L10	NC
L11	NC
L12	NC
L13	NC
L14	NC
L15	NC
L16	NC
L17	NC
L18	NC
L19	NC
L20	NC
L21	NC
L22	NC
M10	NC
M11	NC
M12	NC
M13	NC
M14	NC
M15	NC
M16	NC
M17	NC
M18	NC
M19	NC
M20	NC
M21	NC
M22	EXT_TS1#
N10	NC
N11	NC
N12	NC
N13	NC
N14	NC
N15	NC
N16	NC
N17	NC
N18	NC
N19	NC
N20	NC
N21	NC
N22	NC
P10	NC
P11	NC
P12	NC
P13	NC
P14	NC
P15	NC
P16	NC
P17	NC

Ball	Signal
P18	NC
P19	NC
P20	NC
P21	NC
P22	NC
R10	NC
R11	NC
R12	NC
R13	NC
R14	NC
R18	NC
R19	NC
R20	NC
R21	NC
R22	NC
T11	NC
T12	NC
T13	NC
T14	NC
T18	NC
T19	NC
T20	NC
T21	NC
U10	NC
U11	NC
U12	NC

Ball	Signal
U13	NC
U14	NC
U18	NC
U19	NC
U20	NC
U21	NC
U22	NC
V10	NC
V11	NC
V12	NC
V13	NC
V14	NC
V15	NC
V16	NC
V17	NC
V18	NC
V19	NC
V20	NC
V21	NC
V22	NC
W10	NC
W11	NC
W12	NC
W13	NC
W14	NC
W15	NC
W16	NC

Ball	Signal
W17	NC
W18	NC
W19	NC
W20	NC
W21	NC
W22	NC
Y10	NC
Y11	NC
Y12	NC
Y13	NC
Y14	NC
Y15	NC
Y16	NC
Y17	NC
Y18	NC
Y19	NC
Y20	NC
Y21	NC
Y22	NC

Table *13-53*. Configuration & Reserved Signal Group

Ball	Signal
D15	CFG0
E17	CFG1
F15	CFG2

Ball	Signal
G17	CFG5
H17	CFG6
H19	RSVD23

Ball	Signal
F29	RSVD24
E27	RSVD25
W2	RSVD1

Table 13-54. Voltage Reference and Compensation Signal Groups

Ball	Signal Name
System Memory	
AB27	SMOCDCOMP0
AE9	SMOCDCOMP1
AD7	SMRCOMPN
AE7	SMRCOMPP
Y24	SMXSLEWIN
AA25	SMXSLEWOUT
AC10	SMYSLEWIN
AD10	SMYSLEWOUT
Y30	SMVREF0
AE1	SMVREF1

Ball	Signal Name
Host Interface	
K1	HXRCOMP
E6	HXSCOMP
J13	HXSWING
L1	HYRCOMP
K2	HYSCOMP
L3	HYSWING
J11	HVREF
SDVO	
P26	EXP_COMPI

Ball	Signal Name
L26	EXP_ICOMPO
CRT DAC	
J21	REFSET
TV	
J19	TV_REFSET
LVDS	
J29	LVREFH
H29	LVREFL
F30	LIBG
G30	LVBG

Table 13-55. Power Signal Group

Ball	Signal
PLL Signal Group	
AD1	VCCA_HPLL
AC1	VCCA_MPLL
AC3	VCCD_HMPLL1
AC5	VCCD_HMPLL2
R23	VCCA_3GPLL
B21	VCCA_DPLLA
J30	VCCA_DPLLB
PCI Express Graphics	
P31	VCC3G
R31	VCC3G
M31	VCCA_3GBG
L31	VSSA_3GBG
High Voltage	
B20	VCCHV

Ball	Signal
C21	VCCHV
C22	VCCHV
CRT DAC	
H21	VCC_SYNC
C20	VCCA_CRTDAC
D21	VCCA_CRTDAC
D20	VSSA_CRTDAC
LVDS Signal Group	
A23	VCCD_LVDS
B23	VCCD_LVDS
B25	VCCD_LVDS
A26	VCCTX_LVDS
B26	VCCTX_LVDS
B29	VCCA_LVDS

Ball	Signal
B30	VSSALVDS
TV Out Signal Group	
E18	VCCD_TVDAC
D17	VCCDQ_TVDAC
F18	VCCA_TVDACA
G18	VCCA_TVDACA
F19	VCCA_TVDACB
G19	VCCA_TVDACB
F20	VCCA_TVDACC
G20	VCCA_TVDACC
E19	VCCA_TVBG
E20	VSSA_TVBG

Table 13-56. System Memory Analog Power Signal Group

Ball	Signal
AC13	VCCASM
AC14	VCCASM
AL15	VCCASM

Table 13-57. System Memory Power Signal Group

Ball	Signal
AD18	VCCSM
AE17	VCCSM
AE18	VCCSM
AF1	VCCSM
AF17	VCCSM
AF18	VCCSM
AH17	VCCSM
AH18	VCCSM
AJ17	VCCSM

Ball	Signal
AJ18	VCCSM
AK17	VCCSM
AK18	VCCSM
AK30	VCCSM
AL17	VCCSM
AL18	VCCSM
AL23	VCCSM
AL6	VCCSM
AG17	VCCSM

Ball	Signal
AG18	VCCSM
AC17	VCCSM
AC18	VCCSM
AC31	VCCSM
AD17	VCCSM

Table 13-58. VTT Power Signal Group

Ball	Signal
A6	VTT
A12	VTT
E1	VTT
M1	VTT
M2	VTT
M3	VTT
M4	VTT
M5	VTT
M6	VTT
M7	VTT
M8	VTT
M9	VTT
N1	VTT
N2	VTT
N3	VTT
N4	VTT
N5	VTT
N6	VTT
N7	VTT
N8	VTT
N9	VTT
Y1	VTT

Table 13-59. GMCH Core Voltage Power Signal Group

Ball	Signal
L23	VCC
L24	VCC
M24	VCC
N23	VCC
N24	VCC
P24	VCC
R15	VCC
R17	VCC
T15	VCC
T16	VCC
T17	VCC
U16	VCC

Table 13-60. GMCH Ground Signal Group

Ball	Signal
A15	VSS
A18	VSS
A20	VSS
A25	VSS
A27	VSS
AA2	VSS
AA23	VSS
AA26	VSS
AA27	VSS
AA7	VSS
AB28	VSS
AB30	VSS
AC24	VSS
AC28	VSS
AC9	VSS
AD12	VSS
AD15	VSS
AD19	VSS
AD2	VSS
AD21	VSS
AD5	VSS
AD9	VSS
AE10	VSS
AE11	VSS
AE13	VSS
AE26	VSS
AE30	VSS
AF11	VSS

Ball	Signal
AF15	VSS
AF19	VSS
AF23	VSS
AF28	VSS
AF30	VSS
AF7	VSS
AG2	VSS
AG21	VSS
AG25	VSS
AG3	VSS
AH10	VSS
AH13	VSS
AH15	VSS
AH19	VSS
AH6	VSS
AJ27	VSS
AJ3	VSS
AK12	VSS
AK15	VSS
AK19	VSS
AK21	VSS
AK23	VSS
AK26	VSS
AK29	VSS
AK5	VSS
AK9	VSS
B12	VSS
B15	VSS

Ball	Signal
B22	VSS
B27	VSS
B4	VSS
B6	VSS
B9	VSS
C15	VSS
C17	VSS
C19	VSS
C2	VSS
C25	VSS
C30	VSS
C8	VSS
D11	VSS
D14	VSS
D18	VSS
D19	VSS
D25	VSS
E15	VSS
E21	VSS
E23	VSS
E26	VSS
E29	VSS
E30	VSS
E4	VSS
E7	VSS
F12	VSS
F17	VSS
F23	VSS

Ball	Signal
F27	VSS
G15	VSS
G2	VSS
G21	VSS
G22	VSS
G25	VSS
G29	VSS
G31	VSS
G6	VSS
G8	VSS
H11	VSS
H13	VSS
H18	VSS
H20	VSS
H23	VSS
H26	VSS
H30	VSS
J17	VSS
J20	VSS
J22	VSS
J4	VSS
L2	VSS
L25	VSS
L27	VSS
L29	VSS
L4	VSS
L6	VSS

Ball	Signal
L8	VSS
M23	VSS
M25	VSS
M27	VSS
M29	VSS
N25	VSS
N27	VSS
N29	VSS
N31	VSS
P2	VSS
P23	VSS
P25	VSS
P27	VSS
P29	VSS
P4	VSS
P6	VSS
P8	VSS
R16	VSS
R24	VSS
R25	VSS
R26	VSS
R27	VSS
R29	VSS
U15	VSS
U17	VSS
U23	VSS
U25	VSS

Ball	Signal
U27	VSS
U29	VSS
U31	VSS
U4	VSS
U7	VSS
V1	VSS
V25	VSS
V27	VSS
V28	VSS
V30	VSS
V8	VSS
W24	VSS
W26	VSS
W28	VSS
W30	VSS
W6	VSS
Y23	VSS
Y25	VSS
Y26	VSS
Y29	VSS
Y31	VSS
Y4	VSS
Y9	VSS

13.4.1 Mobile Intel 915GMS Express Chipset Family Ball-Out Numerical Order Ball List

Ball	Signal
A10	NC
A11	HA10#
A12	VTT
A13	HA14#
A14	HA22#
A15	VSS
A17	TVDAC_A
A18	VSS
A19	TVDAC_C
A2	NC
A20	VSS
A21	DREF_CLKP
A22	DREF_CLKN
A23	VCCD_LVDS
A25	VSS
A26	VCCTX_LVDS
A27	VSS
A29	NC
A3	NC
A30	NC
A31	NC
A4	HDRDY#
A5	HRS0#
A6	VTT
A7	HREQ3#
A8	HREQ0#
A9	HREQ2#
AA1	HD57#
AA10	NC
AA11	NC
AA12	NC
AA13	NC
AA14	NC
AA15	NC
AA16	NC
AA17	NC
AA18	NC
AA19	NC
AA2	VSS
AA20	NC

Ball	Signal
AA21	NC
AA22	NC
AA23	VSS
AA24	SA_MA9
AA25	SMXSLEWOUT
AA26	VSS
AA27	VSS
AA28	SA_DQ4
AA29	SA_DQ5
AA3	HCLKN
AA30	SA_DQS0#
AA31	SA_DM0
AA4	HDSTBN3#
AA5	HDSTBP3#
AA6	HD59#
AA7	VSS
AA8	HD56#
AA9	HD55#
AB1	NC
AB10	NC
AB11	NC
AB12	NC
AB13	NC
AB14	NC
AB15	NC
AB17	NC
AB18	NC
AB19	NC
AB2	NC
AB20	NC
AB21	NC
AB22	NC
AB23	SA_MA11
AB24	SA_MA12
AB25	SA_BS2
AB26	SA_RCVENOUT#
AB27	SMOCDCOMP0
AB28	VSS
AB29	SA_DQS0
AB3	NC

Ball	Signal
AB30	VSS
AB31	SA_DQ6
AB5	NC
AB6	NC
AB7	NC
AB9	NC
AC1	VCCA_MPLL
AC10	SMYSLEWIN
AC11	SA_MA10
AC12	SB_MA0
AC13	VCCA_SM
AC14	VCCA_SM
AC15	SB_MA2
AC17	VCCSM
AC18	VCCSM
AC19	SA_MA2
AC2	SA_DQ63
AC20	SA_MA1
AC21	SA_MA0
AC22	NC
AC23	SM_CKE0
AC24	VSS
AC25	SM_CKE1
AC26	SA_DQ23
AC27	SA_RCVENIN#
AC28	VSS
AC29	SA_DQ2
AC3	VCCD_HMPLL1
Ac30	SA_DQ7
AC31	VCCSM
AC5	VCCD_HMPLL2
AC6	SA_DQ58
AC7	SA_DQ59
AC9	VSS
AD1	VCCA_HPLL
AD10	SMYSLEWOUT
AD11	SM_CS0#
AD12	VSS
AD13	SA_BS1
AD14	SB_MA3

Ball	Signal
AD15	VSS
AD17	VCCSM
AD18	VCCSM
AD19	VSS
AD2	VSS
AD20	SA_MA3
AD21	VSS
AD3	SA_DQ62
AD5	VSS
AD6	SA_DM7
AD7	SMRCOMPN
AD9	VSS
AE1	SMVREF1
AE10	VSS
AE11	VSS
AE12	SA_CAS#
AE13	VSS
AE14	SB_MA1
AE15	SA_BS0
AE17	VCCSM
AE18	VCCSM
AE19	SA_MA4
AE2	SA_DQS7
AE20	SA_MA5
AE21	SA_MA8
AE22	NC
AE23	SA_DQ22
AE24	SA_DQ19
AE25	SA_DQ18
AE26	VSS
AE27	SA_DQ20
AE28	SA_DQ17
AE29	SA_DQ3
AE3	SA_DQ61
AE30	VSS
AE31	SM_CK0
AE5	SM_CK1#
AE6	SA_DQ47
AE7	SMRCOMPP
AE9	SMOCDCOMP1
AF1	VCCSM
AF10	SA_DQ41
AF11	VSS
AF12	SM_ODT0
AF13	SA_MA13

Ball	Signal
AF14	SB_MA10
AF15	VSS
AF17	VCCSM
AF18	VCCSM
AF19	VSS
AF2	SA_DQS7#
AF20	SA_MA6
AF21	SA_MA7
AF22	NC
AF23	VSS
AF24	SA_DM2
AF25	SA_DQS2
AF26	SA_DQS2#
AF27	SA_DQ21
AF28	VSS
AF29	SA_DQ16
AF3	SA_DQ60
AF30	VSS
AF31	SM_CK0#
AF5	SM_CK1
AF6	SA_DQ43
AF7	VSS
AF9	SA_DQS5#
AG1	SA_DQ57
AG10	SA_DQ40
AG11	SA_DQ45
AG12	SM_ODT1
AG13	SM_CS1#
AG14	SB_BS1
AG15	SA_RAS#
AG17	VCCSM
AG18	VCCSM
AG19	SB_MA4
AG2	VSS
AG20	SB_MA12
AG21	VSS
AG22	NC
AG23	SA_DQ30
AG24	SA_DQ31
AG25	VSS
AG26	SA_DQ27
AG27	SA_DQ26
AG28	SA_DQ9
AG29	SA_DQ8
AG3	VSS

Ball	Signal
AG30	SA_DQ12
AG31	SA_DQ13
AG5	SA_DQS6#
AG6	SA_DQ46
AG7	SA_DM5
AG9	SA_DQS5
AH1	SA_DQ56
AH10	VSS
AH11	SA_DQ44
AH12	SM_CS3#
AH13	VSS
AH14	SB_RAS#
AH15	VSS
AH17	VCCSM
AH18	VCCSM
AH19	VSS
AH2	SA_DQ55
AH20	SB_MA9
AH21	SM_CKE2
AH3	SA_DQS6
AH5	SM_CK4
AH6	VSS
AH7	SA_DQ42
AH9	SA_DQ38
AJ1	NC
AJ10	SA_DM4
AJ11	SA_DQ37
AJ12	SM_ODT3
AJ13	SB_CAS#
AJ14	SB_BS0
AJ15	SA_WE#
AJ17	VCCSM
AJ18	VCCSM
AJ19	SB_MA5
AJ2	SA_DQ51
AJ20	SB_MA6
AJ21	SM_CKE3
AJ22	NC
AJ23	SA_DQS3
AJ24	SA_DQS3#
AJ25	SA_DQ25
AJ26	SA_DQ10
AJ27	VSS
AJ28	SM_CK3#
AJ29	SM_CK3

Ball	Signal
AJ3	VSS
AJ30	SA_DM1
AJ31	NC
AJ5	SM_CK4#
AJ6	SA_DQ53
AJ7	SA_DQ34
AJ9	SA_DQ39
AK1	NC
AK10	SA_DQS4
AK11	SA_DQ32
AK12	VSS
AK13	SM_ODT2
AK14	SB_WE#
AK15	VSS
AK17	VCCSM
AK18	VCCSM
AK19	VSS
AK2	SA_DQ50
AK20	SB_MA7
AK21	VSS
AK22	NC
AK23	VSS
AK24	SA_DM3
AK25	SA_DQ28
AK26	VSS
AK27	SA_DQ15
AK28	SA_DQS1#
AK29	VSS
AK3	SA_DQ54
AK30	VCCSM
AK31	NC
AK5	VSS
AK6	SA_DQ52
AK7	SA_DQ49
AK9	VSS
AL1	NC
AL10	SA_DQS4#
AL11	SA_DQ33
AL12	SA_DQ36
AL13	SB_MA13
AL14	SM_CS2#
AL15	VCCA_SM
AL17	VCCSM
AL18	VCCSM
AL19	SB_MA8

Ball	Signal
AL2	NC
AL20	SB_MA11
AL21	SB_BS2
AL22	NC
AL23	VCCSM
AL24	SA_DQ29
AL25	SA_DQ24
AL26	SA_DQ11
AL27	SA_DQ14
AL28	SA_DQS1
AL29	NC
AL3	NC
AL30	NC
AL31	NC
AL5	SA_DM6
AL6	VCCSM
AL7	SA_DQ48
AL9	SA_DQ35
B1	NC
B10	NC
B11	HA8#
B12	VSS
B13	HA21#
B14	HA31#
B15	VSS
B17	TV_IRTNA
B18	TV_IRTNB
B19	TV_IRTNC
B2	HHIT#
B20	VCCHV
B21	VCCA_DPLLA
B22	VSS
B23	VCCD_LVDS
B25	VCCD_LVDS
B26	VCCTX_LVDS
B27	VSS
B29	VCCA_LVDS
B3	HBPRI#
B30	VSSALVDS
B31	NC
B4	VSS
B5	HRS1#
B6	VSS
B7	HREQ1#
B8	HA6#

Ball	Signal
B9	VSS
C1	NC
C10	NC
C11	HA7#
C12	HA15#
C13	HA23#
C14	HA27#
C15	VSS
C17	VSS
C18	TVDAC_B
C19	VSS
C2	VSS
C20	VCCA_CRTDAC
C21	VCCHV
C22	VCCHV
C23	BLUE#
C25	VSS
C26	LCTLB_DATA
C27	LACLKP
C29	LADATAP2
C3	HHITM#
C30	VSS
C31	NC
C4	HLOCK#
C5	HCPUSLP#
C6	HA3#
C7	HRS2#
C8	VSS
C9	HA9#
D11	VSS
D12	HA11#
D13	HA30#
D14	VSS
D15	CFG0
D17	VCCDQ_TVDAC
D18	VSS
D19	VSS
D20	VSSA_CRTDAC
D21	VCCA_CRTDAC
D22	GREEN#
D23	BLUE
D25	VSS
D26	LCTLA_CLK
D27	LACLKN
D29	LADATAN2

Ball	Signal
D30	LADATAP1
D31	LADATAN1
E1	VTT
E10	NC
E11	HA13#
E12	HA5#
E13	HA26#
E14	HA29#
E15	VSS
E17	CFG1
E18	VCCD_TVDAC
E19	VCCA_TVBG
E2	HD2#
E20	VSSA_TVBG
E21	VSS
E22	GREEN
E23	VSS
E25	LDDC_CLK
E26	VSS
E27	RSVD25
E29	VSS
E3	HD7#
E30	VSS
E31	LADATAP0
E4	VSS
E5	HDEFER#
E6	HXSCOMP
E7	VSS
E8	HBNR#
E9	HTRDY#
F1	HD13#
F10	NC
F11	HADSTB0#
F12	VSS
F13	HA12#
F14	HA28#
F15	CFG2
F17	VSS
F18	VCCA_TVDACA
F19	VCCA_TVDACB
F2	HD1#
F20	VCCA_TVDACC
F21	RED
F22	RED#
F23	VSS

Ball	Signal
F25	LDDC_DATA
F26	LBKLT_EN
F27	VSS
F29	RSVD24
F3	HD4#
F30	LIBG
F31	LADATAN0
F4	HD6#
F5	HD0#
F6	HD9#
F7	HCPURST#
F8	HDBSY#
F9	HBREQ0#
G1	HDPWR#
G10	NC
G11	HA4#
G12	HA16#
G13	HA19#
G14	HA17#
G15	VSS
G17	CFG5
G18	VCCA_TVDACA
G19	VCCA_TVDACB
G2	VSS
G20	VCCA_TVDACC
G21	VSS
G22	VSS
G23	VSYNC
G25	VSS
G26	LBKLT_CRTL
G27	SDVOCTRL_CLK
G29	VSS
G3	HD5#
G30	LVBG
G31	VSS
G4	HDSTBP0#
G5	HDSTBN0#
G6	VSS
G7	HD15#
G8	VSS
G9	HADS#
H11	VSS
H12	HA25#
H13	VSS
H14	HA20#

Ball	Signal
H15	HADSTB1#
H17	CFG6
H18	VSS
H19	RSVD23
H20	VSS
H21	VCC_SYNC
H22	HSYNC
H23	VSS
H25	LVDD_EN
H26	VSS
H27	SDVOCTRL_DATA
H29	LVREFL
H30	VSS
H31	DREF_SSCLKN
J1	HD12#
J10	CFG12
J11	HVREF
J12	HREQ4#
J13	HXSWING
J14	HA18#
J15	HA24#
J17	VSS
J18	THRMTRIP#
J19	TV_REFSET
J2	HD22#
J20	VSS
J21	REFSET
J22	VSS
J23	DDCCLK
J25	DDCDATA
J26	BM_BUSY#
J27	EXT_TS0#
J29	LVREFH
J3	HD21#
J30	VCCA_DPLLB
J31	DREF_SSCLKP
J4	VSS
J5	HD3#
J6	HDINV0#
J7	HD10#
J8	HD11#
J9	HD8#
K1	HXRCOMP
K10	NC
K11	NC

Ball	Signal
K12	NC
K13	NC
K14	NC
K15	NC
K17	NC
K18	NC
K19	NC
K2	HYSCOMP
K20	NC
K21	NC
K22	NC
K23	NC
K25	NC
K26	NC
K27	NC
K29	NC
K3	HD16#
K30	NC
K31	NC
K4	HD17#
K5	HD20#
K6	HD29#
K7	HD25#
K8	HDSTBN1#
K9	HD14#
L1	HYRCOMP
L10	NC
L11	NC
L12	NC
L13	NC
L14	NC
L15	NC
L16	NC
L17	NC
L18	NC
L19	NC
L2	VSS
L20	NC
L21	NC
L22	NC
L23	VCC
L24	VCC
L25	VSS
L26	EXP_ICOMPO
L27	VSS

Ball	Signal
L28	SDVO_TVCLKIN
L29	VSS
L3	HYSWING
L30	SDVOB_RED
L31	VSSA_3GBG
L4	VSS
L5	HD23#
L6	VSS
L7	HDINV1#
L8	VSS
L9	HDSTBP1#
M1	VTT
M10	NC
M11	NC
M12	NC
M13	NC
M14	NC
M15	NC
M16	NC
M17	NC
M18	NC
M19	NC
M2	VTT
M20	NC
M21	NC
M22	EXT_TS1#
M23	VSS
M24	VCC
M25	VSS
M26	SDVOB_GREEN
M27	VSS
M28	SDVO_TVCLKIN#
M29	VSS
M3	VTT
M30	SDVOB_RED#
M31	VCCA_3GBG
M4	VTT
M5	VTT
M6	VTT
M7	VTT
M8	VTT
M9	VTT
N1	VTT
N10	NC
N11	NC

Ball	Signal
N12	NC
N13	NC
N14	NC
N15	NC
N16	NC
N17	NC
N18	NC
N19	NC
N2	VTT
N20	NC
N21	NC
N22	NC
N23	VCC
N24	VCC
N25	VSS
N26	SDVOB_GREEN#
N27	VSS
N28	SDVOB_INT
N29	VSS
N3	VTT
N30	SDVOB_BLUE
N31	VSS
N4	VTT
N5	VTT
N6	VTT
N7	VTT
N8	VTT
N9	VTT
P1	HD18#
P10	NC
P11	NC
P12	NC
P13	NC
P14	NC
P15	NC
P16	NC
P17	NC
P18	NC
P19	NC
P2	VSS
P20	NC
P21	NC
P22	NC
P23	VSS
P24	VCC

Ball	Signal
P25	VSS
P26	EXP_COMPI
P27	VSS
P28	SDVOB_INT#
P29	VSS
P3	HD36#
P30	SDVOB_BLUE#
P31	VCC3G
P4	VSS
P5	HD35#
P6	VSS
P7	HD38#
P8	VSS
P9	HD39#
R1	HD28#
R10	NC
R11	NC
R12	NC
R13	NC
R14	NC
R15	VCC
R16	VSS
R17	VCC
R18	NC
R19	NC
R2	HD19#
R20	NC
R21	NC
R22	NC
R23	VCCA_3GPLL
R24	VSS
R25	VSS
R26	VSS
R27	VSS
R28	SDVO_FLDSTALL
R29	VSS
R3	HD42#
R30	SDVOB_BLKP
R31	VCC3G
R4	HD41#
R5	HD43#
R6	HD34#
R7	HDINV2#
R8	HD37#
R9	HD31#

Ball	Signal
T11	NC
T12	NC
T13	NC
T14	NC
T15	VCC
T16	VCC
T17	VCC
T18	NC
T19	NC
T20	NC
T21	NC
U1	HDSTBN2#
U10	NC
U11	NC
U12	NC
U13	NC
U14	NC
U15	VSS
U16	VCC
U17	VSS
U18	NC
U19	NC
U2	HDSTBP2#
U20	NC
U21	NC
U22	NC
U23	VSS
U24	DMI_RXP0
U25	VSS
U26	DMI_TXP0
U27	VSS
U28	SDVO_FLDSTALL#
U29	VSS
U3	HD30#
U30	SDVOB_BLKN
U31	VSS
U4	VSS
U5	HD45#
U6	HD44#
U7	VSS
U8	HD24#
U9	HD26#
V1	VSS
V10	NC
V11	NC

Ball	Signal
V12	NC
V13	NC
V14	NC
V15	NC
V16	NC
V17	NC
V18	NC
V19	NC
V2	HD51#
V20	NC
V21	NC
V22	NC
V23	GCLKN
V24	DMI_RXN0
V25	VSS
V26	DMI_TXN0
V27	VSS
V28	VSS
V29	DMI_RXP1
V3	HD32#
V30	VSS
V31	DMI_TXP1
V4	HD33#
V5	HD46#
V6	HD47#
V7	HD58#
V8	VSS
V9	HD27#
W1	HD50#
W10	NC
W11	NC
W12	NC
W13	NC
W14	NC
W15	NC
W16	NC
W17	NC
W18	NC
W19	NC
W2	RSVD1
W20	NC
W21	NC
W22	NC
W23	GCLKP
W24	VSS

Ball	Signal
W25	RSTIN#
W26	VSS
W27	PWROK
W28	VSS
W29	DMI_RXN1
W3	HD40#
W30	VSS
W31	DMI_TXN1
W4	HD52#
W5	HDINV3#
W6	VSS
W7	HD48#
W8	HD49#
W9	HD62#
Y1	VTT
Y10	NC
Y11	NC
Y12	NC

Ball	Signal
Y13	NC
Y14	NC
Y15	NC
Y16	NC
Y17	NC
Y18	NC
Y19	NC
Y2	HD53#
Y20	NC
Y21	NC
Y22	NC
Y23	VSS
Y24	SMXSLEWIN
Y25	VSS
Y26	VSS
Y27	SA_DQ0
Y28	SA_DQ1
Y29	VSS

Ball	Signal
Y3	HCLKP
Y30	SMVREF0
Y31	VSS
Y4	VSS
Y5	HD54#
Y6	HD60#
Y7	HD63#
Y8	HD61#
Y9	VSS

13.5 Mobile Intel 915GMS Express Chipset Family Signal Name Ordering Ball List

Ball	Signal
D23	BLUE
C23	BLUE#
J26	BM_BUSY#
D15	CFG0
E17	CFG1
F15	CFG2
G17	CFG5
H17	CFG6
J23	DDCCLK
J25	DDCDATA
V24	DMI_RXN0
W29	DMI_RXN1
U24	DMI_RXP0
V29	DMI_RXP1
V26	DMI_TXN0
W31	DMI_TXN1
U26	DMI_TXP0
V31	DMI_TXP1
A22	DREF_CLKN
A21	DREF_CLKP
H31	DREF_SSCLKN
J31	DREF_SSCLKP
P26	EXP_COMPI
L26	EXP_ICOMPO
M28	SDVO_TVCLKIN#
P28	SDVOB_INT#
U28	SDVO_FLDSTALL#
L28	SDVO_TVCLKIN
N28	SDVOB_INT
R28	SDVO_FLDSTALL
M30	SDVOB_RED#
N26	SDVOB_GREEN#
P30	SDVOB_BLUE#
U30	SDVOB_BLKN
L30	SDVOB_RED
M26	SDVOB_GREEN
N30	SDVOB_BLUE
R30	SDVOB_BLKP
J27	EXT_TS0#

Ball	Signal
M22	EXT_TS1#
V23	GCLKN
W23	GCLKP
E22	GREEN
D22	GREEN#
A11	HA10#
D12	HA11#
F13	HA12#
E11	HA13#
A13	HA14#
C12	HA15#
G12	HA16#
G14	HA17#
J14	HA18#
G13	HA19#
H14	HA20#
B13	HA21#
A14	HA22#
C13	HA23#
J15	HA24#
H12	HA25#
E13	HA26#
C14	HA27#
F14	HA28#
E14	HA29#
C6	HA3#
D13	HA30#
B14	HA31#
G11	HA4#
E12	HA5#
B8	HA6#
C11	HA7#
B11	HA8#
C9	HA9#
G9	HADS#
F11	HADSTB0#
H15	HADSTB1#
E8	HBNR#
B3	HBPRI#

Ball	Signal
F9	HBREQ0#
AA3	HCLKN
Y3	HCLKP
F7	HCPURST#
C5	HCPUSLP#
F5	HD0#
F2	HD1#
J7	HD10#
J8	HD11#
J1	HD12#
F1	HD13#
K9	HD14#
G7	HD15#
K3	HD16#
K4	HD17#
P1	HD18#
R2	HD19#
E2	HD2#
K5	HD20#
J3	HD21#
J2	HD22#
L5	HD23#
U8	HD24#
K7	HD25#
U9	HD26#
V9	HD27#
R1	HD28#
K6	HD29#
J5	HD3#
U3	HD30#
R9	HD31#
V3	HD32#
V4	HD33#
R6	HD34#
P5	HD35#
P3	HD36#
R8	HD37#
P7	HD38#
P9	HD39#

Ball	Signal
F3	HD4#
W3	HD40#
R4	HD41#
R3	HD42#
R5	HD43#
U6	HD44#
U5	HD45#
V5	HD46#
V6	HD47#
W7	HD48#
W8	HD49#
G3	HD5#
W1	HD50#
V2	HD51#
W4	HD52#
Y2	HD53#
Y5	HD54#
AA9	HD55#
AA8	HD56#
AA1	HD57#
V7	HD58#
AA6	HD59#
F4	HD6#
Y6	HD60#
Y8	HD61#
W9	HD62#
Y7	HD63#
E3	HD7#
J9	HD8#
F6	HD9#
F8	HDBSY#
E5	HDEFER#
J6	HDINV0#
L7	HDINV1#
R7	HDINV2#
W5	HDINV3#
G1	HDPWR#
A4	HDRDY#
G5	HDSTBN0#
K8	HDSTBN1#
U1	HDSTBN2#
AA4	HDSTBN3#
G4	HDSTBP0#
L9	HDSTBP1#
U2	HDSTBP2#

Ball	Signal
AA5	HDSTBP3#
B2	HHIT#
C3	HHITM#
C4	HLOCK#
A8	HREQ0#
B7	HREQ1#
A9	HREQ2#
A7	HREQ3#
J12	HREQ4#
A5	HRS0#
B5	HRS1#
C7	HRS2#
H22	HSYNC
E9	HTRDY#
J11	HVREF
K1	HXRCOMP
E6	HXSCOMP
J13	HXSWING
L1	HYRCOMP
K2	HYSCOMP
L3	HYSWING
D27	LACLKN
C27	LACLKP
F31	LADATAN0
D31	LADATAN1
D29	LADATAN2
E31	LADATAP0
D30	LADATAP1
C29	LADATAP2
G26	LBKLT_CRTL
F26	LBKLT_EN
D26	LCTLA_CLK
C26	LCTLB_DATA
E25	LDDC_CLK
F25	LDDC_DATA
F30	LIBG
G30	LVBG
H25	LVDD_EN
J29	LVREFH
H29	LVREFL
A10	NC
A31	NC
AA10	NC
AA11	NC
AA12	NC

Ball	Signal
AA13	NC
AA14	NC
AA15	NC
AA16	NC
AA17	NC
AA18	NC
AA19	NC
AA20	NC
AA21	NC
AA22	NC
AB1	NC
AB10	NC
AB11	NC
AB12	NC
AB13	NC
AB14	NC
AB15	NC
AB17	NC
AB18	NC
AB19	NC
AB2	NC
AB20	NC
AB21	NC
AB22	NC
AB3	NC
AB5	NC
AB6	NC
AB7	NC
AB9	NC
AC22	NC
AE22	NC
AF22	NC
AG22	NC
AJ22	NC
AK22	NC
AL22	NC
B10	NC
C10	NC
E10	NC
F10	NC
G10	NC
J10	NC
K10	NC
K11	NC
K12	NC

Ball	Signal
K13	NC
K14	NC
K15	NC
K17	NC
K18	NC
K19	NC
K20	NC
K21	NC
K22	NC
K23	NC
K25	NC
K27	NC
K29	NC
K30	NC
K31	NC
L10	NC
L11	NC
L12	NC
L13	NC
L14	NC
L15	NC
L16	NC
L17	NC
L18	NC
L19	NC
L20	NC
L21	NC
M11	NC
M12	NC
M13	NC
M14	NC
M15	NC
M16	NC
M17	NC
M18	NC
M19	NC
M20	NC
M21	NC
N10	NC
N11	NC
N12	NC
N13	NC
N14	NC
N15	NC
N16	NC

Ball	Signal
N17	NC
N18	NC
N19	NC
N20	NC
N21	NC
N22	NC
P10	NC
P11	NC
P12	NC
P13	NC
P14	NC
P15	NC
P16	NC
P17	NC
P18	NC
P19	NC
P20	NC
P21	NC
P22	NC
R10	NC
R11	NC
R12	NC
R13	NC
R14	NC
R18	NC
R19	NC
R20	NC
R21	NC
R22	NC
T11	NC
T12	NC
T13	NC
T14	NC
T18	NC
T19	NC
T20	NC
T21	NC
U10	NC
U11	NC
U12	NC
U13	NC
U14	NC
U18	NC
U19	NC
U20	NC

Ball	Signal
U21	NC
U22	NC
V10	NC
V11	NC
V12	NC
V13	NC
V14	NC
V15	NC
V16	NC
V17	NC
V18	NC
V19	NC
V20	NC
V21	NC
V22	NC
W10	NC
W11	NC
W12	NC
W13	NC
W14	NC
W15	NC
W16	NC
W17	NC
W18	NC
W19	NC
W20	NC
W21	NC
W22	NC
Y10	NC
Y11	NC
Y12	NC
Y13	NC
Y14	NC
Y15	NC
Y16	NC
Y17	NC
Y18	NC
Y19	NC
Y20	NC
Y21	NC
Y22	NC
AL31	NC
AK31	NC
AJ31	NC
C31	NC

Ball	Signal
B31	NC
AL30	NC
A30	NC
AL29	NC
A2	NC
B1	NC
A29	NC
AL3	NC
A3	NC
AL2	NC
AL1	NC
AK1	NC
AJ1	NC
C1	NC
W27	PWROK
F21	RED
F22	RED#
J21	REFSET
W25	RSTIN#
W2	RSVD1
K26	NC
L22	NC
H19	RSVD23
F29	RSVD24
E27	RSVD25
M10	NC
F10	NC
AE15	SA_BS0
AD13	SA_BS1
AB25	SA_BS2
AE12	SA_CAS#
AA31	SA_DM0
AJ30	SA_DM1
AF24	SA_DM2
AK24	SA_DM3
AJ10	SA_DM4
AG7	SA_DM5
AL5	SA_DM6
AD6	SA_DM7
Y27	SA_DQ0
Y28	SA_DQ1
AJ26	SA_DQ10
AL26	SA_DQ11
AG30	SA_DQ12
AG31	SA_DQ13

Ball	Signal
AL27	SA_DQ14
AK27	SA_DQ15
AF29	SA_DQ16
AE28	SA_DQ17
AE25	SA_DQ18
AE24	SA_DQ19
AC29	SA_DQ2
AE27	SA_DQ20
AF27	SA_DQ21
AE23	SA_DQ22
AC26	SA_DQ23
AL25	SA_DQ24
AJ25	SA_DQ25
AG27	SA_DQ26
AG26	SA_DQ27
AK25	SA_DQ28
AL24	SA_DQ29
AE29	SA_DQ3
AG23	SA_DQ30
AG24	SA_DQ31
AK11	SA_DQ32
AL11	SA_DQ33
AJ7	SA_DQ34
AL9	SA_DQ35
AL12	SA_DQ36
AJ11	SA_DQ37
AH9	SA_DQ38
AJ9	SA_DQ39
AA28	SA_DQ4
AG10	SA_DQ40
AF10	SA_DQ41
AH7	SA_DQ42
AF6	SA_DQ43
AH11	SA_DQ44
AG11	SA_DQ45
AG6	SA_DQ46
AE6	SA_DQ47
AL7	SA_DQ48
AK7	SA_DQ49
AA29	SA_DQ5
AK2	SA_DQ50
AJ2	SA_DQ51
AK6	SA_DQ52
AJ6	SA_DQ53
AK3	SA_DQ54

Ball	Signal
AH2	SA_DQ55
AH1	SA_DQ56
AG1	SA_DQ57
AC6	SA_DQ58
AC7	SA_DQ59
AB31	SA_DQ6
AF3	SA_DQ60
AE3	SA_DQ61
AD3	SA_DQ62
AC2	SA_DQ63
Ac30	SA_DQ7
AG29	SA_DQ8
AG28	SA_DQ9
AB29	SA_DQS0
AA30	SA_DQS0#
AL28	SA_DQS1
AK28	SA_DQS1#
AF25	SA_DQS2
AF26	SA_DQS2#
AJ23	SA_DQS3
AJ24	SA_DQS3#
AK10	SA_DQS4
AL10	SA_DQS4#
AG9	SA_DQS5
AF9	SA_DQS5#
AH3	SA_DQS6
AG5	SA_DQS6#
AE2	SA_DQS7
AF2	SA_DQS7#
AC21	SA_MA0
AC20	SA_MA1
AC11	SA_MA10
AB23	SA_MA11
AB24	SA_MA12
AF13	SA_MA13
AC19	SA_MA2
AD20	SA_MA3
AE19	SA_MA4
AE20	SA_MA5
AF20	SA_MA6
AF21	SA_MA7
AE21	SA_MA8
AA24	SA_MA9
AG15	SA_RAS#
AC27	SA_RCVENIN#

Ball	Signal
AB26	SA_RCVENOUT#
AJ15	SA_WE#
AJ14	SB_BS0
AG14	SB_BS1
AL21	SB_BS2
AJ13	SB_CAS#
AC12	SB_MA0
AE14	SB_MA1
AF14	SB_MA10
AL20	SB_MA11
AG20	SB_MA12
AL13	SB_MA13
AC15	SB_MA2
AD14	SB_MA3
AG19	SB_MA4
AJ19	SB_MA5
AJ20	SB_MA6
AK20	SB_MA7
AL19	SB_MA8
AH20	SB_MA9
AH14	SB_RAS#
AK14	SB_WE#
G27	SDVOCTRL_CLK
H27	SDVOCTRL_DATA
AE31	SM_CK0
AF31	SM_CK0#
AF5	SM_CK1
AE5	SM_CK1#
AJ29	SM_CK3
AJ28	SM_CK3#
AH5	SM_CK4
AJ5	SM_CK4#
AC23	SM_CKE0
AC25	SM_CKE1
AH21	SM_CKE2
AJ21	SM_CKE3
AD11	SM_CS0#
AG13	SM_CS1#
AL14	SM_CS2#
AH12	SM_CS3#
AF12	SM_ODT0
AG12	SM_ODT1
AK13	SM_ODT2
AJ12	SM_ODT3
AB27	SMOCDCOMP0

Ball	Signal
AE9	SMOCDCOMP1
AD7	SMRCOMPN
AE7	SMRCOMPP
Y30	SMVREF0
AE1	SMVREF1
Y24	SMXSLEWIN
AA25	SMXSLEWOUT
AC10	SMYSLEWIN
AD10	SMYSLEWOUT
J18	THRMTRIP#
B17	TV_IRTNA
B18	TV_IRTNB
B19	TV_IRTNC
J19	TV_REFSET
A17	TVDAC_A
C18	TVDAC_B
A19	TVDAC_C
L23	VCC
L24	VCC
M24	VCC
N23	VCC
N24	VCC
P24	VCC
R15	VCC
R17	VCC
T15	VCC
T16	VCC
T17	VCC
U16	VCC
H21	VCC_SYNC
P31	VCC3G
R31	VCC3G
M31	VCCA_3GBG
R23	VCCA_3GPLL
C20	VCCA_CRTDAC
D21	VCCA_CRTDAC
B21	VCCA_DPLLA
J30	VCCA_DPLLB
AD1	VCCA_HPLL
B29	VCCA_LVDS
AC1	VCCA_MPLL
AC13	VCCA_SM
AC14	VCCA_SM
AL15	VCCA_SM
E19	VCCA_TVBG

Ball	Signal
F18	VCCA_TVDACA
G18	VCCA_TVDACA
F19	VCCA_TVDACB
G19	VCCA_TVDACB
F20	VCCA_TVDACC
G20	VCCA_TVDACC
AC3	VCCD_HMPLL1
AC5	VCCD_HMPLL2
A23	VCCD_LVDS
B23	VCCD_LVDS
B25	VCCD_LVDS
E18	VCCD_TVDAC
D17	VCCDQ_TVDAC
B20	VCCHV
C21	VCCHV
C22	VCCHV
AC17	VCCSM
AC18	VCCSM
AC31	VCCSM
AD17	VCCSM
AD18	VCCSM
AE17	VCCSM
AE18	VCCSM
AF1	VCCSM
AF17	VCCSM
AF18	VCCSM
AG17	VCCSM
AG18	VCCSM
AH17	VCCSM
AH18	VCCSM
AJ17	VCCSM
AJ18	VCCSM
AK17	VCCSM
AK18	VCCSM
AK30	VCCSM
AL17	VCCSM
AL18	VCCSM
AL23	VCCSM
AL6	VCCSM
A26	VCCTX_LVDS
B26	VCCTX_LVDS
A15	VSS
A18	VSS
A20	VSS
A25	VSS

Ball	Signal
A27	VSS
AA2	VSS
AA23	VSS
AA26	VSS
AA27	VSS
AA7	VSS
AB28	VSS
AB30	VSS
AC24	VSS
AC28	VSS
AC9	VSS
AD12	VSS
AD15	VSS
AD19	VSS
AD2	VSS
AD21	VSS
AD5	VSS
AD9	VSS
AE10	VSS
AE11	VSS
AE13	VSS
AE26	VSS
AE30	VSS
AF11	VSS
AF15	VSS
AF19	VSS
AF23	VSS
AF28	VSS
AF30	VSS
AF7	VSS
AG2	VSS
AG21	VSS
AG25	VSS
AG3	VSS
AH10	VSS
AH13	VSS
AH15	VSS
AH19	VSS
AH6	VSS
AJ27	VSS
AJ3	VSS
AK12	VSS
AK15	VSS
AK19	VSS
AK21	VSS

Ball	Signal
AK23	VSS
AK26	VSS
AK29	VSS
AK5	VSS
AK9	VSS
B12	VSS
B15	VSS
B22	VSS
B27	VSS
B4	VSS
B6	VSS
B9	VSS
C15	VSS
C17	VSS
C19	VSS
C2	VSS
C25	VSS
C30	VSS
C8	VSS
D11	VSS
D14	VSS
D18	VSS
D19	VSS
D25	VSS
E15	VSS
E21	VSS
E23	VSS
E26	VSS
E29	VSS
E30	VSS
E4	VSS
E7	VSS
F12	VSS
F17	VSS
F23	VSS
F27	VSS
G15	VSS
G2	VSS
G21	VSS
G22	VSS
G25	VSS
G29	VSS
G31	VSS
G6	VSS
G8	VSS

Ball	Signal
H11	VSS
H13	VSS
H18	VSS
H20	VSS
H23	VSS
H26	VSS
H30	VSS
J17	VSS
J20	VSS
J22	VSS
J4	VSS
L2	VSS
L25	VSS
L27	VSS
L29	VSS
L4	VSS
L6	VSS
L8	VSS
M23	VSS
M25	VSS
M27	VSS
M29	VSS
N25	VSS
N27	VSS
N29	VSS
N31	VSS
P2	VSS
P23	VSS
P25	VSS
P27	VSS
P29	VSS
P4	VSS
P6	VSS
P8	VSS
R16	VSS
R24	VSS
R25	VSS
R26	VSS
R27	VSS
R29	VSS
U15	VSS
U17	VSS
U23	VSS
U25	VSS
U27	VSS

Ball	Signal
U29	VSS
U31	VSS
U4	VSS
U7	VSS
V1	VSS
V25	VSS
V27	VSS
V28	VSS
V30	VSS
V8	VSS
W24	VSS
W26	VSS
W28	VSS
W30	VSS
W6	VSS
Y23	VSS
Y25	VSS
Y26	VSS
Y29	VSS
Y31	VSS
Y4	VSS
Y9	VSS
A31	NC
L31	VSSA_3GBG
D20	VSSA_CRTDAC
E20	VSSA_TVBG
B30	VSSALVDS
G23	VSYNC
A12	VTT
A6	VTT
E1	VTT
M1	VTT
M2	VTT
M3	VTT
M4	VTT
M5	VTT
M6	VTT
M7	VTT
M8	VTT
M9	VTT
N1	VTT
N2	VTT
N3	VTT
N4	VTT
N5	VTT

Ball	Signal
N6	VTT
N7	VTT
N8	VTT
N9	VTT
Y1	VTT

13.6 Mobile Intel 91xM Series Express Chipset Family Package Mechanical Information

13.6.1 Intel 915PM/GM/GME and 910GML/GMLE Package Mechanical Information

The Intel 915GMCH comes in a Micro-FCBGA package, which is similar to the mobile processor package. The package consists of a silicon die mounted face down on an organic substrate populated with solder balls on the bottom side. Capacitors may be placed in the area surrounding the die. Because the die-side capacitors are electrically conductive, and only slightly shorter than the die height, care should be taken to avoid contacting the capacitors with electrically conductive materials. Doing so may short the capacitors and possibly damage the device or render it inactive.

The use of an insulating material between the capacitors and any thermal solution should be considered to prevent capacitor shorting. An exclusion, or keep out area, surrounds the die and capacitors, and identifies the contact area for the package. Care should be taken to avoid contact with the package inside this area.

The Intel 915 package is a 1257 ball micro-FCBGA. Unless otherwise specified, interpret the dimensions and tolerances in accordance with ASME Y14.5-1994. The dimensions are in millimeters.

Tolerances:

- .X - ± 0.1
- .XX - ± 0.05
- Angles - ± 1.0 degrees
- Package parameters
- Die Size: 395mm x 395mm
- Land metal diameter: 630 microns
- Solder resist opening: 560 microns

Figure 13-5. Mobile Intel 915PM/GM/GME/GL and 910GMLE Express Chipset Package Micro-FCBGA

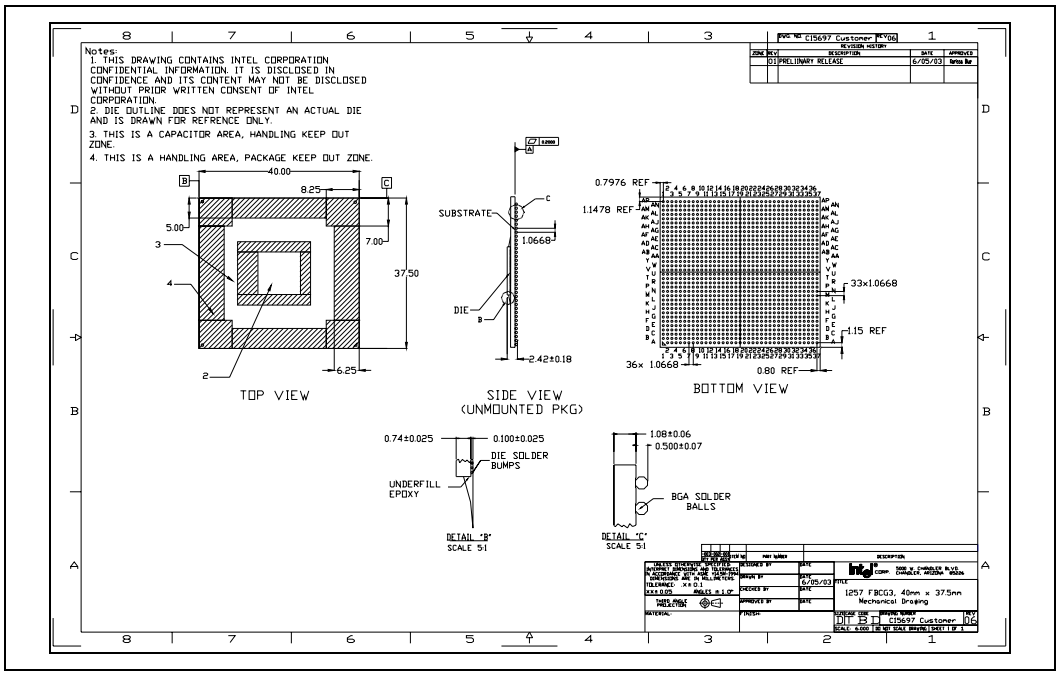


Figure 13-6. Mobile Intel 915PM/GM/GME/GL and 910GMLE Express Chipset Package Ball Grid Array

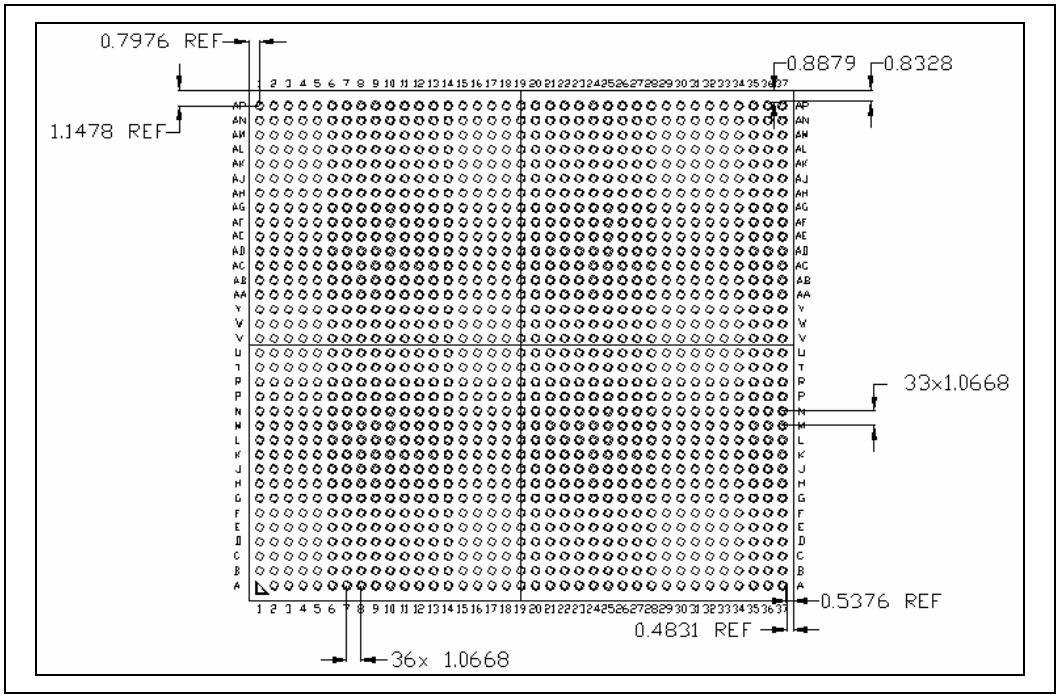


Figure 13-7. Mobile Intel 915PM/GM/GME/GL and 910GMLE Express Chipset Package Top View

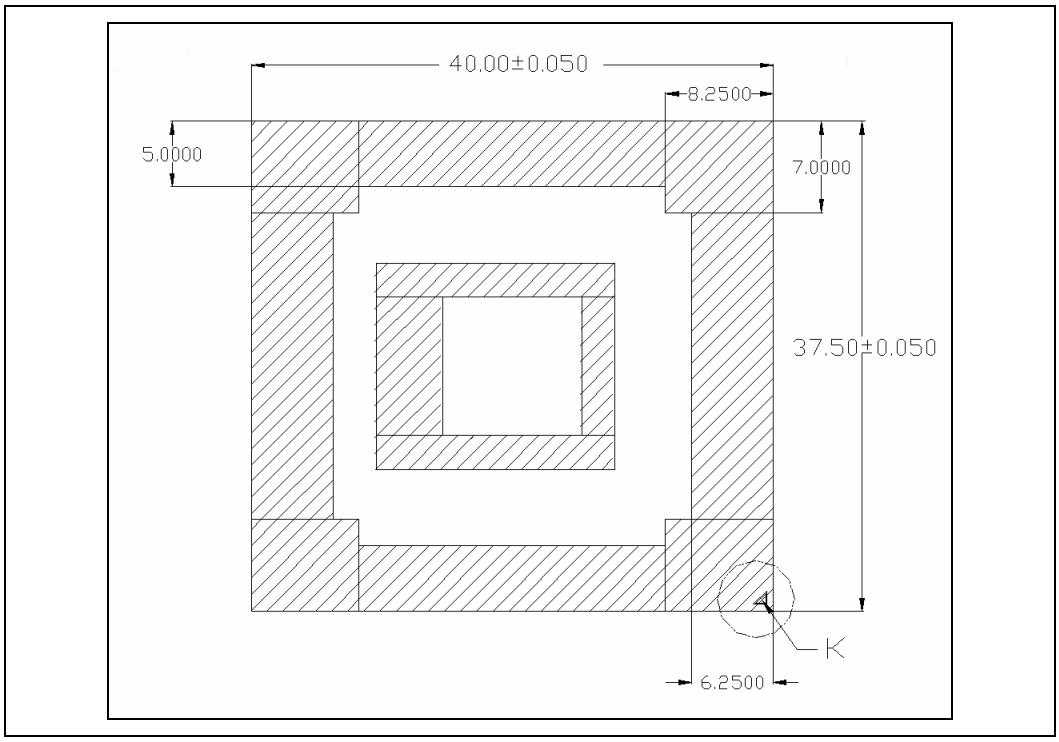


Figure 13-8. Mobile Intel 915PM/GM/GME/GL and 910GMLE Express Chipset Package Side View

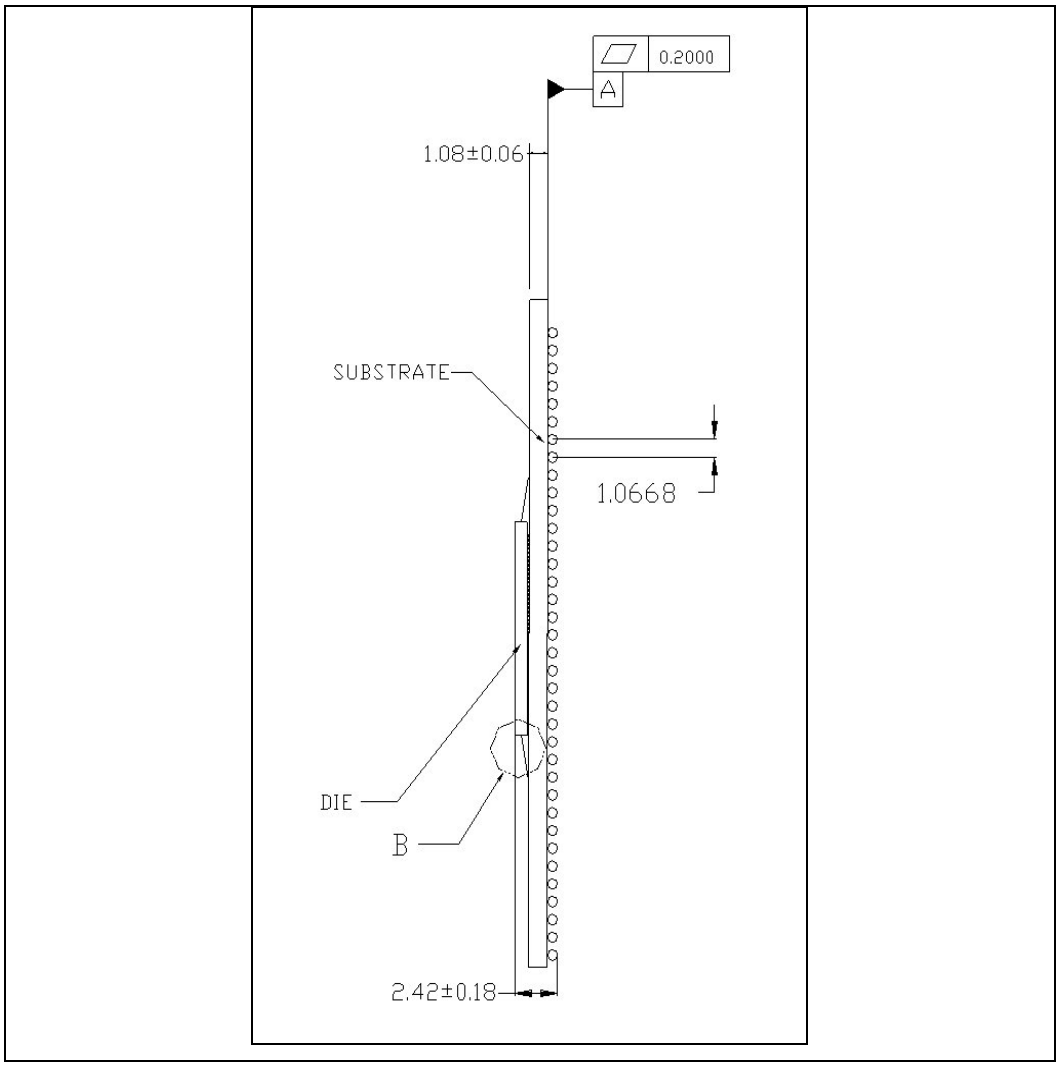


Figure 13-9. Mobile Intel 915PM/GM/GME/GL and 910GMLE Express Chipset Package Details B & K

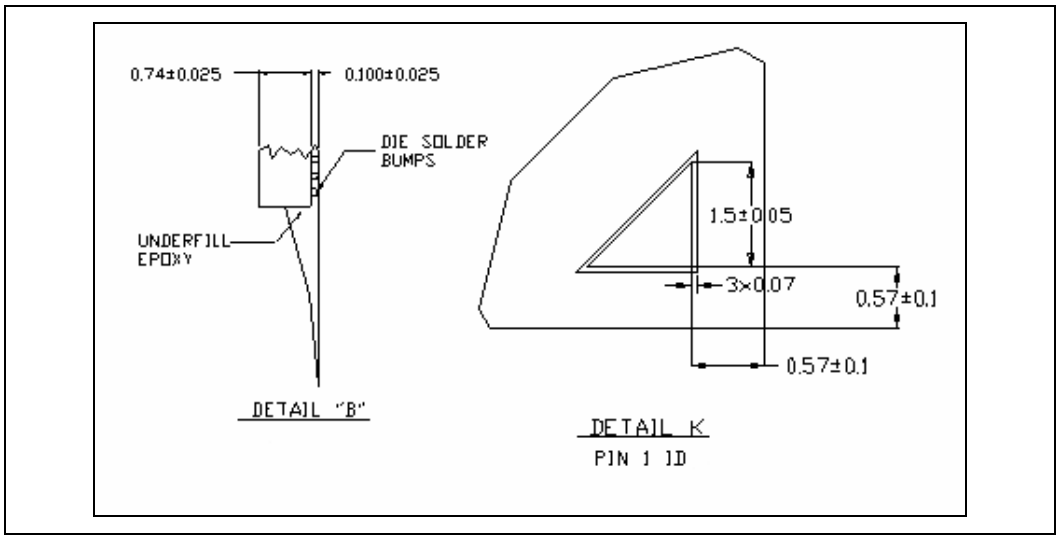
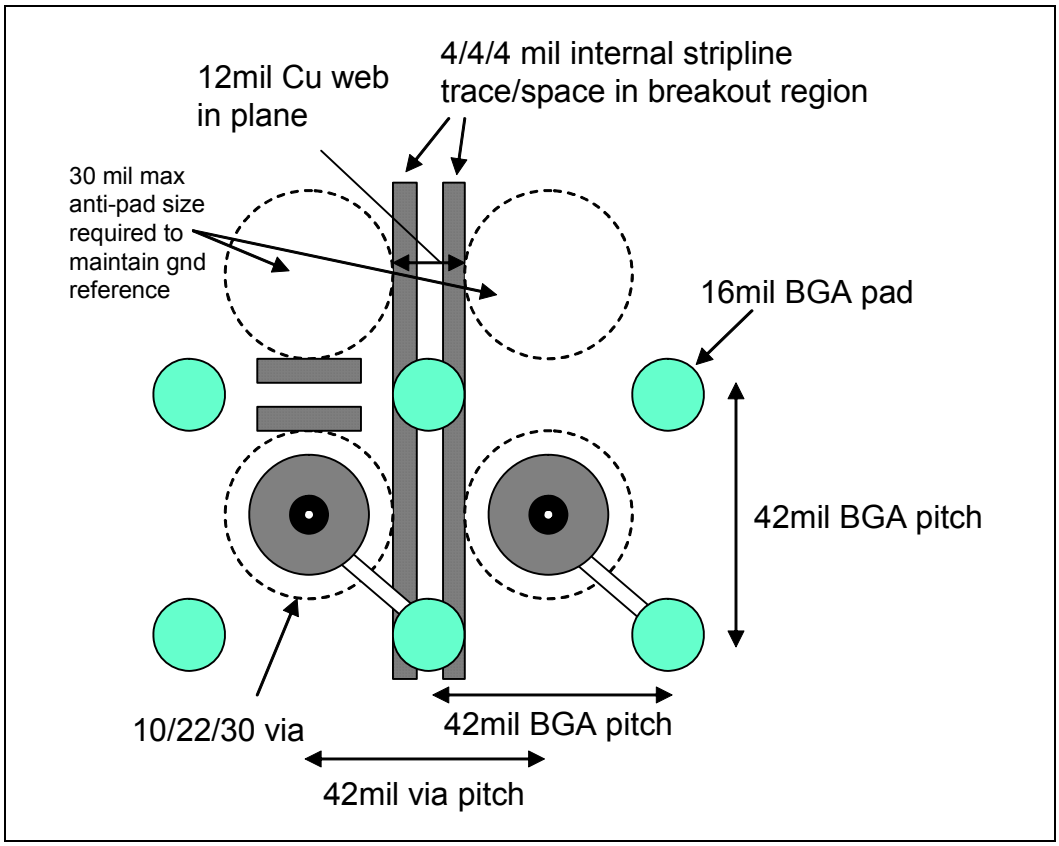


Figure 13-10. Recommended Via Stack Up for Platform (Standard Chipset Package)





13.7 Mobile Intel 915GMS Express Chipset Package Mechanical Information

The Mobile Intel 915GMS Express Chipset comes in a Micro-FCBGA package, which is similar to the mobile processor package. The package consists of a silicon die mounted face down on an organic substrate populated with solder balls on the bottom side. Capacitors may be placed in the area surrounding the die. Because the die-side capacitors are electrically conductive, and only slightly shorter than the die height, care should be taken to avoid contacting the capacitors with electrically conductive materials. Doing so may short the capacitors and possibly damage the device or render it inactive.

The use of an insulating material between the capacitors and any thermal solution should be considered to prevent capacitor shorting. An exclusion, or keep out area, surrounds the die and capacitors, and identifies the contact area for the package. Care should be taken to avoid contact with the package inside this area.

The Intel 915GMS package is an 840 ball micro-FCBGA. Unless otherwise specified, interpret the dimensions and tolerances in accordance with ASME Y14.5-1994. The dimensions are in millimeters.

Tolerances:

- .X - ± 0.1
- .XX - ± 0.05
- Angles - ± 1.0 degrees

Note: The ball array is not uniform and it is non-orthogonal. Mobile Intel 915GMS consists of five regions. Four regions around the periphery and one region in the center. Each region has different pin pitch characteristics to facilitate breakout routing.

Figure 13-11. Mobile Intel 915GMS Express Chipset Package Micro-FCBGA

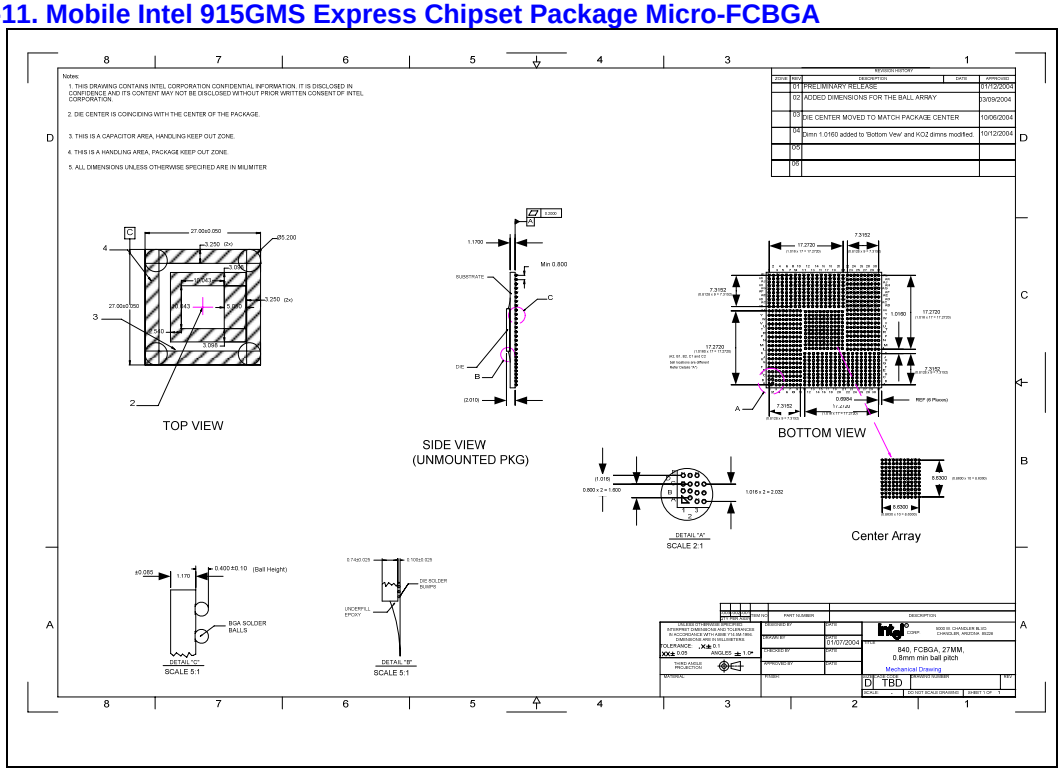
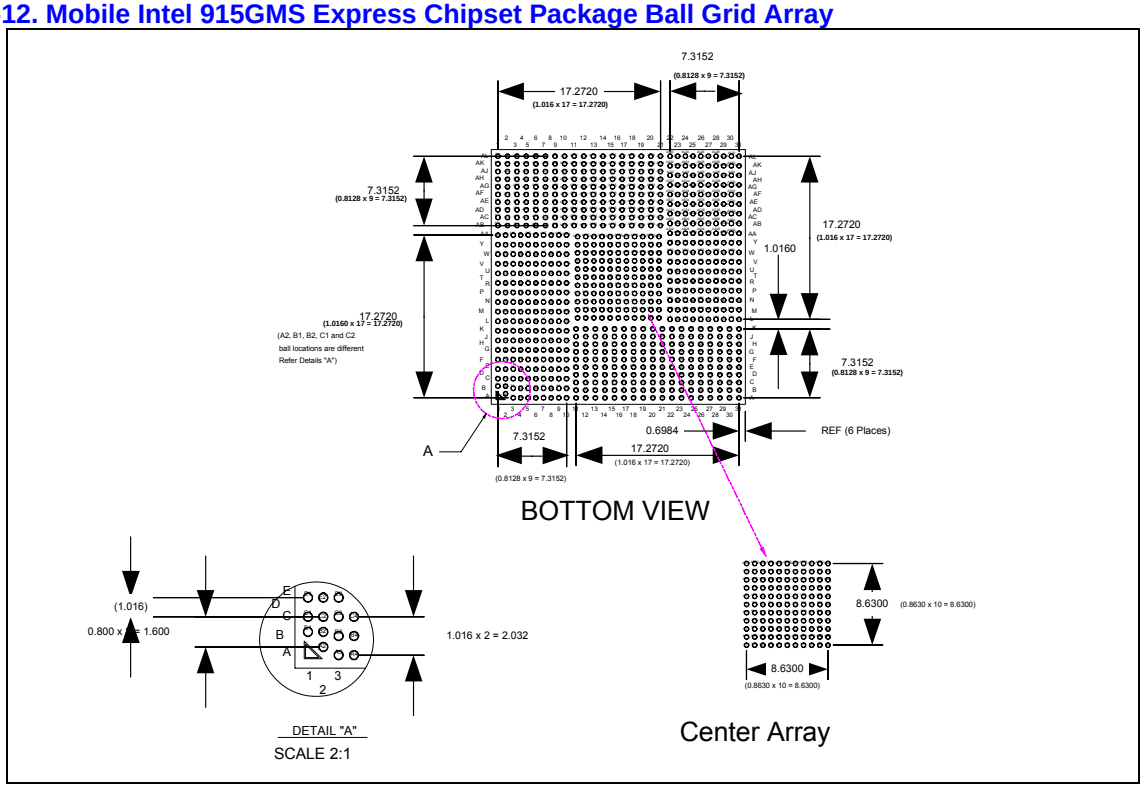


Figure 13-12. Mobile Intel 915GMS Express Chipset Package Ball Grid Array



Note: The center point of the 'center' ball T16 coincides with the center of the package. This should be used as reference for the center ball array.

Figure 13-13. Mobile Intel 915GMS Express Chipset Package Top View

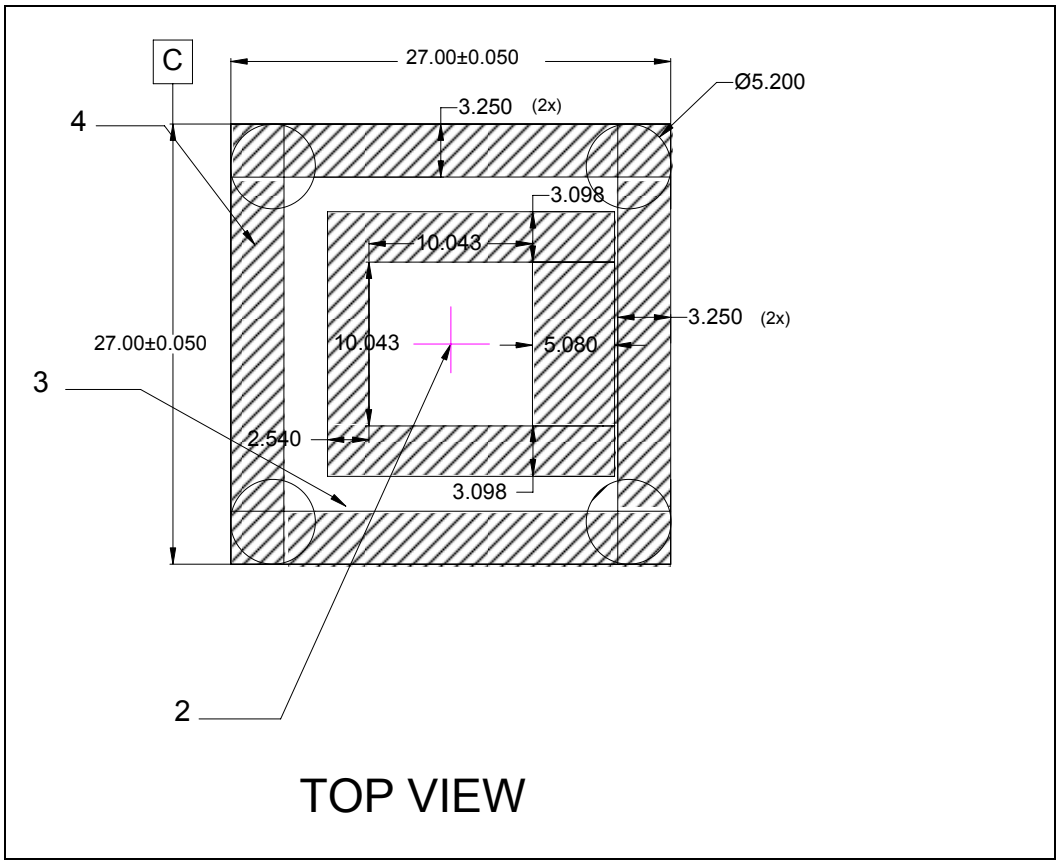


Figure 13-14. Mobile Intel 915GMS Express Chipset Package Side View

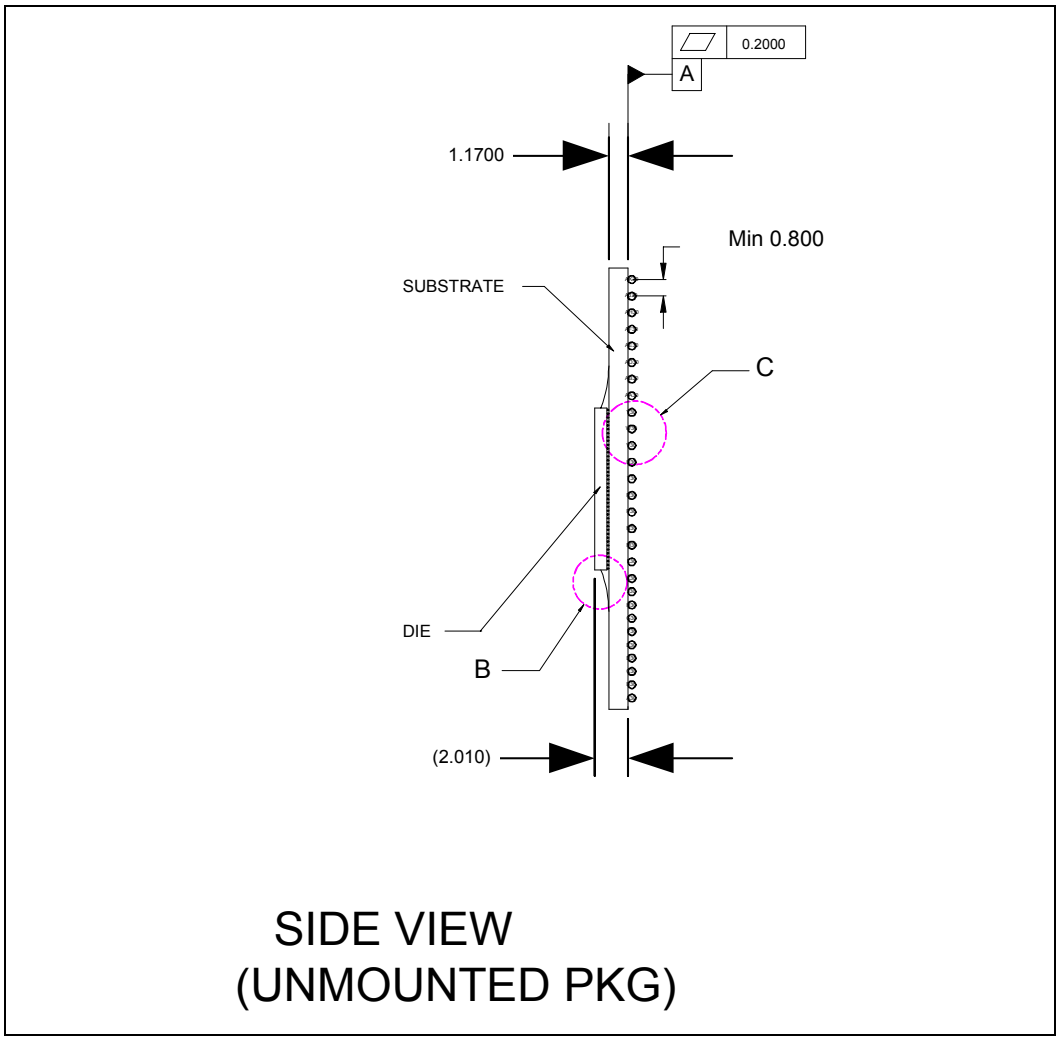


Figure 13-15. Mobile Intel 915GMS Express Chipset Package Details B & C

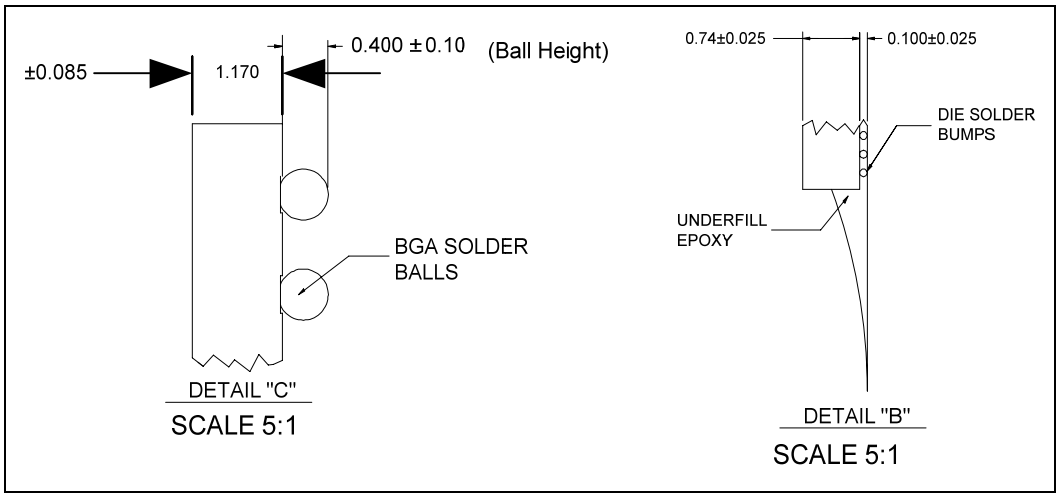
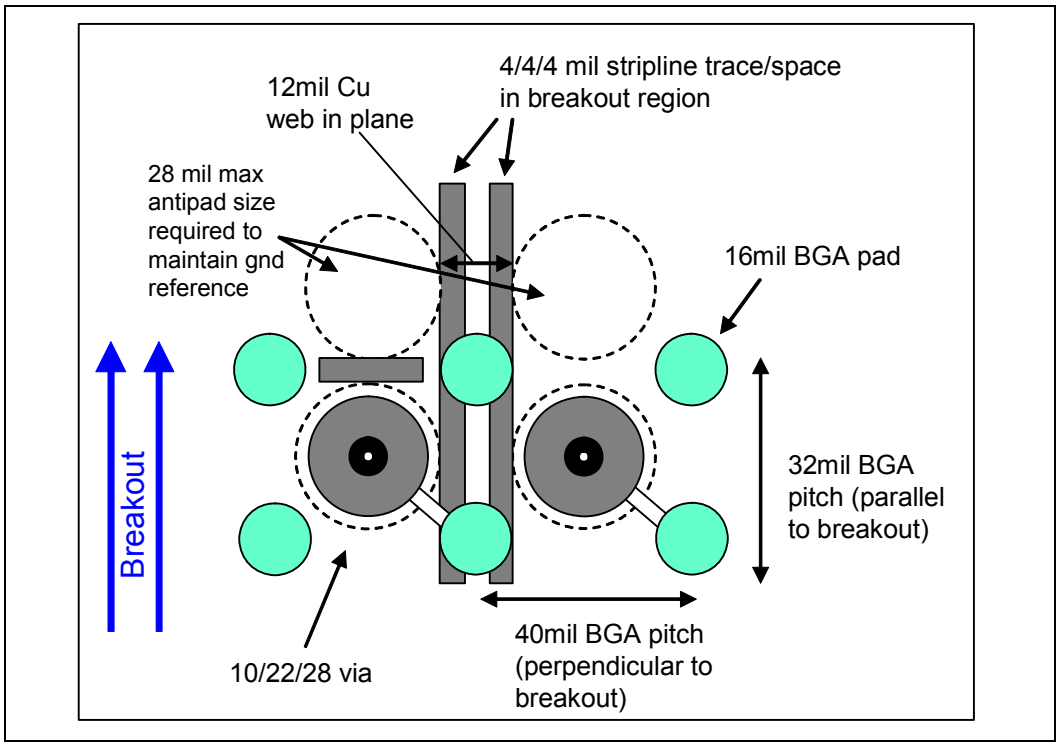


Figure 13-16. Recommended Via Stack Up for Platform (Small Factor Chipset Package)



For the Intel 915GMS, optimal solder joint reliability requires 16-mil diameter pads through out the small form factor board pattern. Reducing pad diameters will have an adverse impact on solder joint reliability and could affect component warrantee.

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